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Introduction

Analog Applications is a collection of analog application notes designed to give readers a basic understanding of TI products and to provide simple but practical examples for typical applications. Written not only for design engineers but also for engineering managers, technicians, system designers and marketing and sales personnel, the book emphasizes general application concepts over lengthy mathematical analyses.

These applications are not intended as "how-to" instructions for specific circuits but as examples of how devices could be used to solve specific design requirements. Readers will find tutorial information as well as practical engineering solutions on components from the following product categories:

- Data Acquisition
- Power Management
- Data Transmission
- Amplifiers

Where applicable, readers will also find software routines and program structures. Finally, *Analog Applications* includes helpful hints and rules of thumb to guide readers in preparing for their design.

Because this book is limited in size, readers should refer to more detailed technical information, which can be found on TI's product-specific websites listed at the bottom of each application note.

Aspects of data acquisition system design

By Perry Miller
Application Specialist, Data Converters

Analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) play an important role in the design of data acquisition systems. ADCs are used to convert analog signals like the output from a temperature transducer, a radio receiver or a video camera into digital signals for processing. Conversely, DACs are used to convert digital signals back to analog signals. For example, the DAC accepts a digital video signal and outputs analog video to drive a monitor CRT, video amplifier or LCD monitor display. Convenience, cost, power dissipation, resolution, speed, supply voltage and ease of use drive the selection of a particular ADC/DAC. Ideally, designers will select an appropriate low-power serial or parallel input CMOS DAC, apply data and control signals to the device and have differential or single-ended analog outputs. Similarly, the requirements for low-power CMOS ADCs include being able to connect single-ended or differential input and control signals to the device and have accurate digital data at the output. It turns out that this is a non-trivial issue because of the wide range of input signals.

Signal processing challenges

A composite video signal has negative horizontal and vertical synchronization signals. The signal level must be shifted before applying it to the input of a CMOS ADC operating with a +5-V AVDD supply if the intent is to digitize the video and synchronization signals. In radio communication systems the analog input signal is buried deep in noise, and interference signals from an adjacent channels can interfere with the in-band RF signal. To help maintain signal quality, modern radio communications systems use a digital receiver to process the RF input. A typical digital receiver circuit chain (see Figure 1) consists of an antenna, a low-noise amplifier (LNA), RF unit, bandpass filter, an ADC, a digital mixer, a decimating low-pass filter, a digital signal processor (DSP) and a DAC connected to an audio amplifier. The ADC is used to bring the RF signal into the digital domain for processing by the DSP. This application note provides a functional specification for designing analog-to-digital converter data acquisition systems.

Common ADC architectures

The common ADC architectures include successive approximation register (SAR), dual-slope, sigma-delta, flash, semi-flash and pipeline.

SAR and dual-slope

The SAR and dual-slope architectures are mainly used in applications requiring high resolution (10 to 22 bits) and low conversion speed in the range of 100 sps (samples per second) to 2 Msps. The SAR converter is the most popular general-purpose ADC and is used in low-to-medium frequency time domain applications. The key to SAR architecture is that it is based on a single comparator. To achieve N bits of resolution, a successive approximation converter must perform N comparator operations, each stored sequentially in the architecture's register. A successive approximation ADC with 12 bits of resolution would execute 12 comparisons on each input signal. An ADC based on a single comparator leads to a very small die size and low power consumption, however, SAR sample

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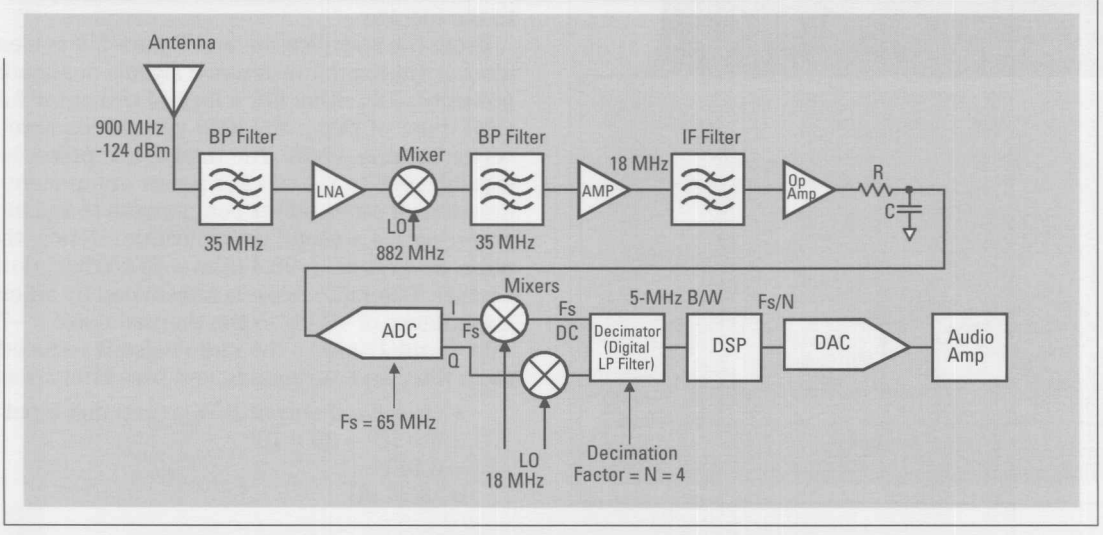
Figure 1. Simplified block diagram of a digital receiver



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rates are inversely proportional to resolution because the conversion method requires one clock cycle to produce each bit of resolution in the output data.

Sigma-delta

The sigma-delta ADC architecture is capable of much higher resolution than the SAR. The typical range is 16 to 24 bits. The tradeoff comes in the form of slower sampling speeds. The sigma delta architecture's sampling speed is limited to approximately 100 ksps. Sigma-delta converters use a technique called oversampling that is based on the theory that a very fast, low-resolution converter can be used to take a large number of samples on an analog signal. The outputs from this oversampling process are then combined into groups, and the groups are averaged using a digital filter like an accumulator-adder. This averaging operation can increase the accuracy of the conversion as long as the input signal does not vary any faster than the sampling rate. This process also eliminates any in-band noise present in the ADC by spreading the noise across the entire sampling frequency band.

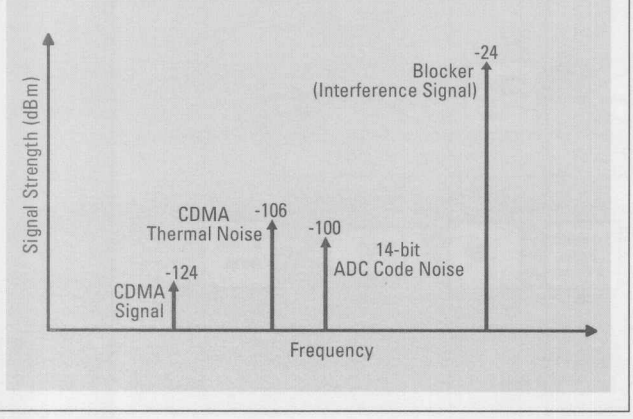
Flash

Flash ADCs are very fast with typical sampling speed ranging from 20 Msps to 800 Msps, with 6- to 8-bit resolution; however, the device power consumption and input capacitance (12 to 30 pF) are high compared to a SAR. The input capacitance issue makes it necessary to drive the flash ADC input with an op amp with very low output impedance. Flash ADCs perform multiple word-at-a-time conversions in parallel. The input signal is connected to a bank of fast comparators. For a flash converter to reach an effective resolution of N bits, the flash architecture must incorporate $2N$-1 comparators. The input capacitance is also very high due to the $2N$-1 comparators in parallel.

Semi-flash

To achieve higher resolutions in the range of 10 to12 bits, a multi-step flash or semi-flash architecture has been developed. This architecture divides the input signal range into a number of sub-ranges through the use of banks of comparators, much like the flash architecture.

Figure 2. CDMA signal and noise power relative to the blocker



Pipeline

Pipeline ADCs are used chiefly for medium- to high-speed conversion in the range of 1 to 80 million samples per second, with resolutions of 8 to 16 bits. A pipeline ADC is made up of n stages + n sampler. Each stage carries out an operation on the input sample and provides the output for the following sampler. Each stage consists of an SHA, an ADC, a DAC, a subtractor and an amplifier. A topic that has received much attention in the last few years is the use of high-speed pipeline ADCs for IF sampling in the implementation of software radio.

System requirements

The starting point for an electronic system design is the specification. Assume that the goal is to process the following code-division multiple-access (CDMA) baseband IF signal:

- 100-dB blocker at 250-kHz at the edge of the pass band
- 4 to 5 bits of resolution in the baseband—translates to an 80-dB spurious-free dynamic range (SFDR)
- An IF signal of 18 MHz (second harmonic from IF at 36 MHz)
- 6- to 12-dB attenuation of second harmonic from op amp
- The digital downconverter has a process gain of 22.4 dB
- The in-band thermal noise power at 25°C is approximately –98.4 dBm
- The sampling rate is 65 MHz
- A radio noise figure of 2 to 4 dB
- An antenna noise bandwidth of 35 MHz
- Eb/No = 5 dB

Selecting the data converter

The in-band thermal noise power

$$Gn = kTB = 1.38 \times 10^{-23} \times 300 \times 35 \times 10^{6}$$

$$= -128.4 \text{ dB or } -98.4 \text{ dBm}$$

where

k = Boltzmann's constant, 1.38×10^{-23} (J/K),
T = temperature (K),
T(K) = T(°C) + 273.15 and
B = equivalent noise bandwidth of the system (Hz).

Figure 2 shows a representation of the power relative to the blocker.

From the specification and Figure 2 it is clear that the blocker (in-band interference signal) dominates the signal power of –124 dBm. For a typical converter full-scale (FS) input of 2Vp-p the RMS voltage required at the converter input is –3 dB. The total signal power is approximately equal to the blocker power component (–3 dB). Relating all other power components to the blocker power makes a useful simplification. Hence, the thermal noise is –77.4 dB (–98.4 dBm + 21.0 dBm) down from the blocker. The radio noise is introduced by adding the radio noise figure of +2 dB to the thermal noise = –75.4 dB. The thermal noise + the radio noise is reduced by the radio filter and decimating low-pass filter by an amount

= (baseband output B/W) ÷ (antenna input B/W)
= $5 \times 10^{6} \div 35 \times 10^{6}$
= 0.143
= –8.45 dB.

The system thermal noise becomes

–75.4 dB – 8.45 dB – 3 dB = –86.85 dB.

As a first cut, use a 14-bit A/D converter with a signal-to-noise ratio (SNR) relative to the received signal power of 76 dB, and the digital downconverter and low-pass filter will reduce the ADC noise by a factor

= (baseband output B/W)÷(A/D converter output B/W)
= $5 \times 10^6 \div (35 \times 10^6 \div 2)$
= $5 \div 32.5$
= 0.154
= –8.13 dB.

Therefore, the new dB down for the ADC is

–76 dB – 8.13 dB – 3 dB = –87.13 dB.*

The total noise

= thermal noise + ADC code noise = –84 dB.

The in-band signal power level relative to –3 dB (full-scale) = –103 dB. The signal-to-noise ratio can be determined from

SNR = –103 dB + 84 dB = –19 dB.

The process gain for Figure 1 is 256 chips/bit or 24 dB. In such a case

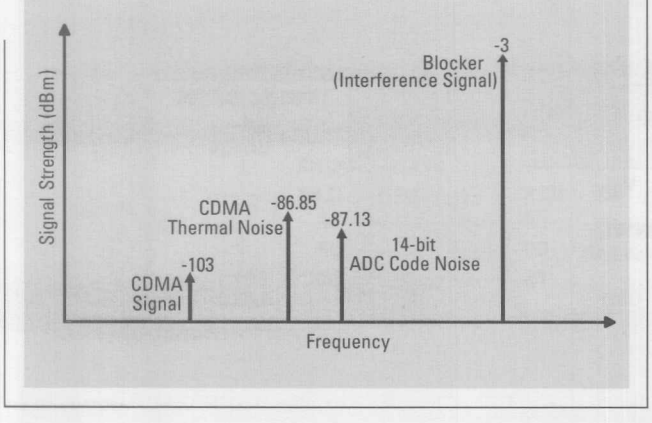
Eb/No = 24 – 19 = 5 dB.

The calculated converter noise is close to the system thermal noise; therefore, a 14-bit A/D converter with a SNR = 76 dB, SFDR = 100 dB, and a sampling rate of 65 Msps is a good choice. Figure 3 shows thermal noise contribution to the band-limited baseband noise.

In the given example of the ADC dynamic performance specifications, how well the pipeline ADC is able to digitize a high-frequency signal is the key for frequency domain applications. Other important dynamic specifications are the signal-to-noise ratio with distortion (SINAD) and effective number of bits (ENOB). Generally, designers should consider these and other performance characteristics such as the type of interface the device presents to the DSP before deciding on the ADC. New CMOS data converters are eliminating many of the compromises designers have faced and some of these devices are able to operate on lower voltages and still provide high throughput and resolution. For example, one such device is the TI THS1265, with12 bits of resolution and a sampling rate of 65 Msps.

*The theoretical SNR of a converter = n bits × 6.02 + 1.76 dB.

Figure 3. CDMA signal and ADC thermal noise contribution to the baseband noise



Interfacing the data converter

Figure 1 illustrates a conventional digital receiver.

Signal conditioning op amp selection

In the type of application shown in Figure 1, the op amps perform the critical function of conditioning signals. The designer must be careful that the op amp does not introduce any additional electrical noise and distortion into the system. As was the case with data converters, a lower voltage level reduces the effective speed of an op amp. This adversely effects the device's output signal slew rate, bandwidth, the settling times and the maximum value of ADCs input capacitance the op amp can drive. An op amp with unity gain 3-dB bandwidth of 450 MHz, SFDR range of 100 to 110 dB, SNR of 90 dB, THD (total harmonic distortion) of –95 dB, slew rate of 1500 V/µs and 40-ns settling time would be a good choice for driving 3 to 15 pF of converter input capacitance. The higher an op amp's slew rate (SR = 2piVpBw), the more accurately the device's output signal will conform to its input signal. An op amp with a fast slew rate means that after a signal transition from high to low or low to high, the signal will transition into its new state quickly with little noise-generating signal bounce. A fast settling time reduces signal bounce following a transition and limits any ringing in the signal. The op amp bandwidth affects the signal phase shift through of the device. The first-order low-pass filter at the output of the op amp is used to attenuate the 18-MHz IF signal second harmonic component by 8 dB. The filter's 3-dB cutoff frequency is set to 20 MHz.

Issues of board layout

Limiting the electrical noise as well as the electromagnetic interference (EMI) on the analog voltage plane of a data acquisition system is always important because ADCs use the supply voltage as a reference point for converting analog waveforms into digital signals. Electrical noise can interfere with the supply voltage and perturb the ADC's reference voltage. One common design mistake is failing to isolate the analog voltage plane from the digital plane. When this happens, the voltage fluctuations in the digital plane can couple to the analog plane and interfere with the accuracy and performance of the system's ADCs. ADCs operate most efficiently from a very clean, steady power supply.

References

1. Andrew J. Veterbi, *CDMA, Principles of Spread Spectrum Communication* (Addison-Wesley, 1997).
2. ITU IMT—2000 Draft Document (CDMA 2000 Draft Document).

Low-power data acquisition sub-system using the TI TLV1572

By Thomas Kugelstadt
Application Manager

With the entrance of the digital signal processor (DSP) into commercial electronic equipment in the late '80s, the number of analog applications turning into digital applications has increased significantly. Technical solutions, previously accomplished using analog circuitry, have been converted into data acquisition systems that translate analog input signals into digital information and process the binary data. In addition, the trend to portable equipment (i.e., PDAs, cellular phones, camcorders) requires electronic circuitry to be smaller and consume less power in order to extend battery life. This application note describes a low-power data acquisition system using the TI TLV1572 10-bit analog-to-digital converter (ADC) and the 16-bit, fixed-point TI TMS320C203 DSP. See Figure 1 for the system block diagram.

The power supply

The system power supply uses the TI TPS7101 adjustable low-voltage dropout regulator (LDO). The device regulates input voltages between 6 to 10 V down to the adjusted output level, providing a typical voltage drop of 32 mV per 100-mA load current. The output voltage is adjusted to 5 V via an external voltage divider consisting of 562-kΩ and 169-kΩ resistors. For an output voltage of 3 V, the 562-kΩ resistor is replaced by a 218-kΩ resistor. The following low-ESR (equivalent series resistance) 4.7-µF solid tantalum capacitor and the 100-nF high-frequency ceramic capacitor are sufficient to ensure stability, provided that the total ESR is maintained between 0.7 Ω and 2.5 Ω. For more information on the selection and type of low-ESR capacitors, refer to the TPS7101 Data Sheet, literature number SLVS092F.

The analog input buffer

The analog input signal is buffered by the TI TLV2772, a fast, low-voltage, low-noise CMOS operational amplifier (op amp). This device operates from 2.2 V to 5.5 V with a typical slew rate of 10.5 V/µs and a typical noise density of 17 nV/√Hz @ 1 kHz. In the configuration shown in Figure 1, the op amp works as a non-inverting amplifier with a gain of two. Before it is amplified, the analog input signal in the range of 0 V to $V_{CC}/2$ is band-limited by the 75-Ω/2.2-nF input low-pass filter. The 100-Ω/3.3-nF low-pass filter at the output reduces the output noise significantly and ensures a signal-to-noise ratio greater than 90 dB at the ADC input.

The analog-to-digital converter

The TLV1572 is a 10-bit, successive approximation ADC operating within a supply voltage range of 2.7 V to 5.5 V. The typical conversion time is ten SCLK cycles with the specified maximum of SCLK = 20 MHz at 4.5-V supply and 10 MHz at 3-V supply. The TLV1572 interfaces easily to DSPs and microcontrollers via a 4-wire serial interface.

Figure 1. Data acquisition sub-system

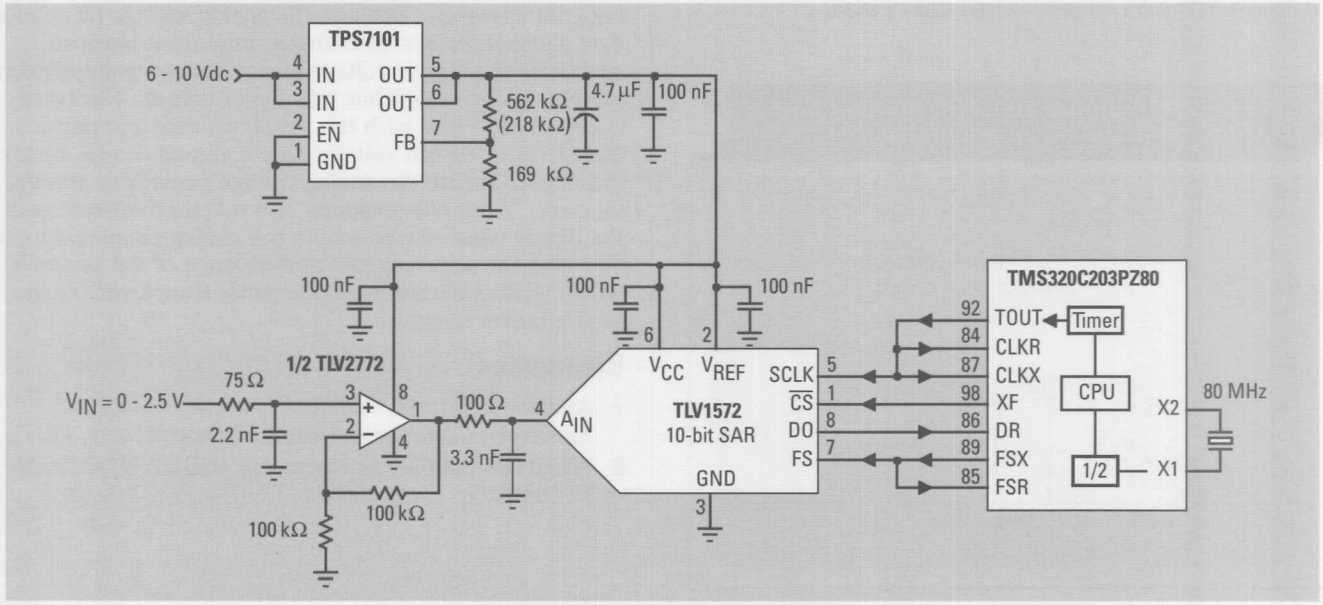
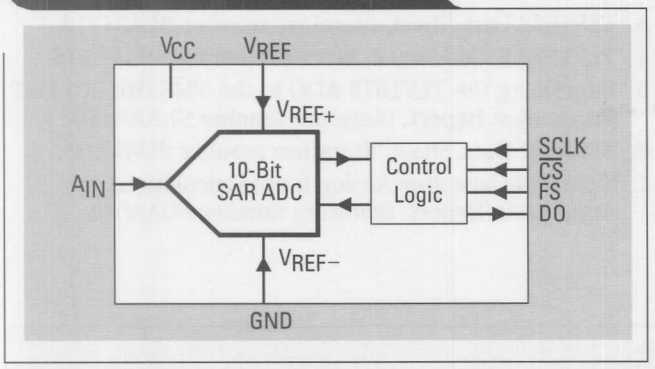


Figure 2. TLV1572 block diagram



The device features an auto-power-down mode that becomes active whenever a conversion is not performed, thus reducing the current consumption to 10 µA.

Figure 2 shows the block diagram of the device. The actual converter employs switched-capacitor architecture to perform successive approximations through charge redistribution. The internal control logic synchronizes the serial interface timing with the sampling and conversion process.

Serial interface timing

Figure 3 shows the interface timing between ADC and DSP. The ADC distinguishes between the µC and DSP modes by checking the frame sync (FS) input level at the falling edge of chip select. If FS is low, DSP mode is set, otherwise the µC mode is set.

With the rising edge of FS, the ADC starts transferring data to the DSP. Six zeros precede the 10-bit result to comply with the 16-bit data format of the DSP. Sampling occurs from the first falling edge of SCLK after FS goes low until the rising edge of SCLK when the sixth zero bit is sent out. Thereafter, decisions are made on the rising edges and data is sent out on the rising edges delayed by 1 bit. The DSP samples on the falling edge of SCLK.

DO goes into 3-state on the 17th rising edge and comes out on a FS rising edge. The device goes into auto-power-down on the 17th falling edge of SCLK. A rising edge of FS pulls it out of power-down and the next data transfer begins.

Interface program

The C-callable assembler routine, which ensures the timely sequence of the interface signals, is shown in Figure 4.

TLV1572START (start assembler routine)

The main program (in C language) starts the assembler routine via a call instruction. All pointers and registers previously used in the C-program are saved and the DSP and its serial port are initialized.

Any user-defined values such as memory start address, number of samples and the used supply voltage are copied from the C-program into the assembler program. The DSP on-chip timer, used as the interface-clock generator, assumes a default value of 10 MHz if a 3-V supply is used. If a 5-V supply is chosen, the timer value is overwritten for 20-MHz operation. Before the actual data transfer starts, the DSP internal receive interrupt flag, RINT, is enabled. The program status flag, END-BIT, which signalizes the exit of the assembler routine, is set to 1. Then the ADC is enabled via its chip-select input. The DSP initiates a data transfer by sending an FS pulse to the ADC, then resides in idle mode and waits for a RINT to occur.

RINT (receive interrupt routine)

On the 16th clock cycle of SCLK, a RINT is generated that forces the CPU to execute the RINT service routine (RINT-ISR). At the beginning of the RINT routine the receive data is stored in the data memory and the memory address is increased by one. The following decision-box decrements the number of samples and checks whether all samples have been received. If all samples were received, the ADC is disabled and the END_BIT is set to zero. Then the timer is stopped and RINT is disabled. The program leaves the RINT-ISR via the EXIT-routine and returns to the C-program. If more samples need to be acquired, the program clears the RINT flag and returns to the Idle-mode where it sends the FS-pulse and stays idle until the next RINT occurs.

Exit 1572 program

As long as END-BIT is set to one, the CPU diverts to the Start-Data-Transfer box to continue acquiring data. Once END_BIT has been set to zero, all previously saved registers in the Save-Context box are restored. The CPU now exits the interface routine and returns to the C-program.

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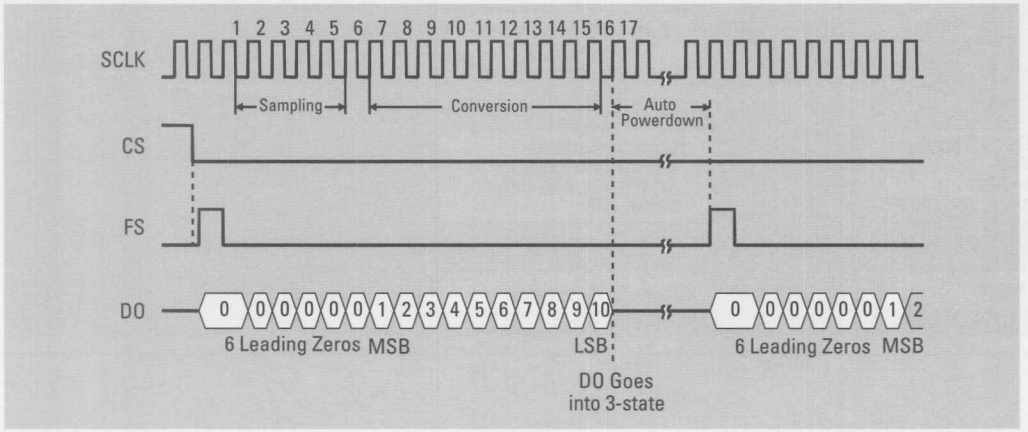
Figure 3. ADC/DSP interface timing



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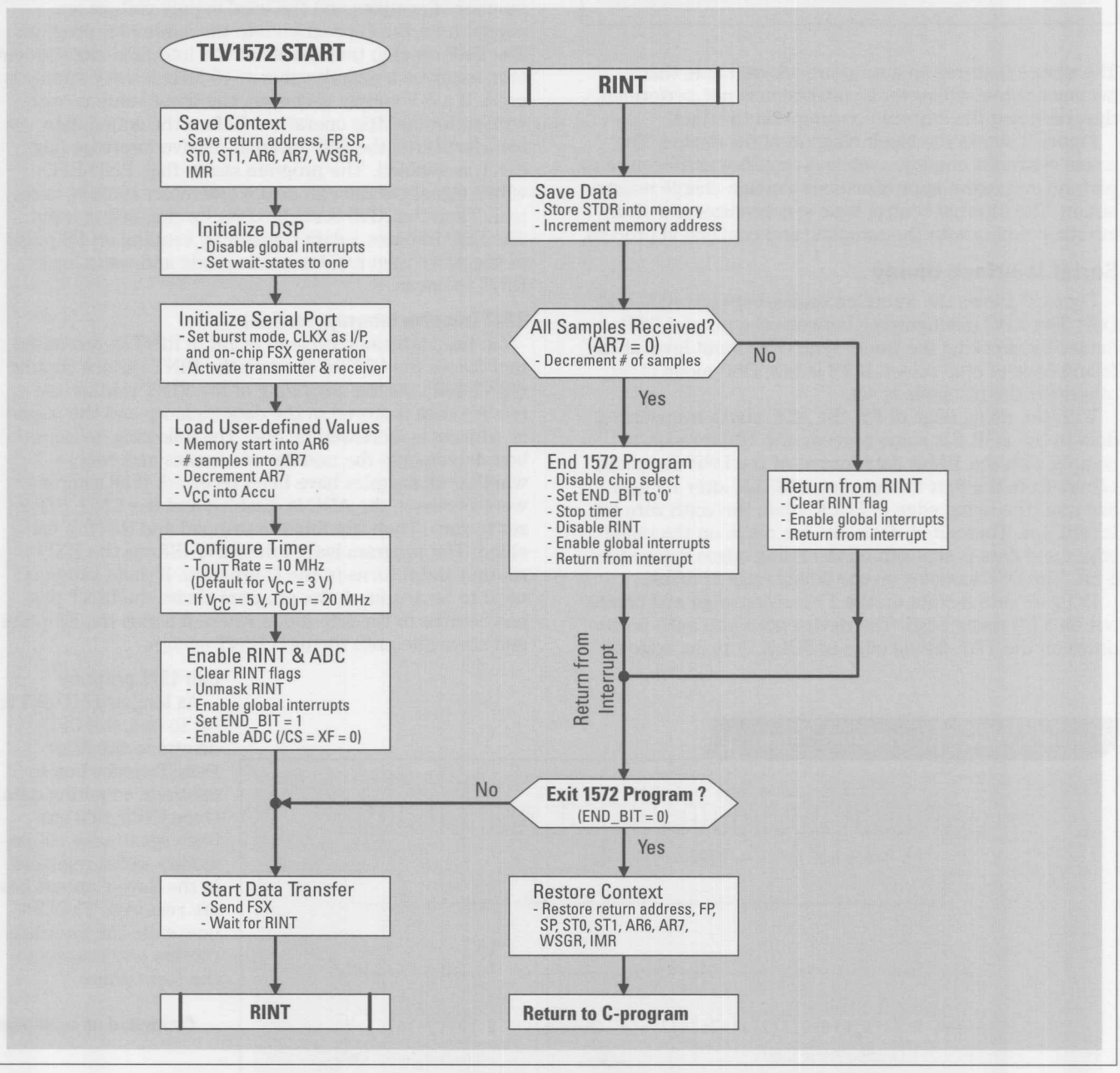
References

For additional information and references, see the following related documents:

1. TMS320C2xx User's Guide, literature number SPRU127B.
2. TMS320C2xx Data Sheet, literature number SPRS025B.
3. TLV1572 Data Sheet, literature number SLAS171A.
4. TLV1572 EVM Manual, literature number SLAU018.
5. Interfacing the TLV1572 ADC to the TMS320C203 DSP Application Report, literature number SLAA026B.
6. TPS7101 Data Sheet, literature number SLVS092F.
7. Switched-Capacitor Analog Input Calculations Application Report, literature number SLAA036.

Figure 4. Flowchart of the interface program



Evaluating operational amplifiers as input amplifiers for A-to-D converters

By James Karki
Application Specialist, Operational Amplifiers

This application note describes a method for comparing the ac performance of the TI TLV2462 and TLV2772 operational amplifiers to the TI TLV2544/TLV2548 analog-to-digital converter. Amplifiers like the TLV2462 and TLV2772 are used to condition the signal input to ADCs (TLV2544/TLV2548). Normally the functions performed include level shifting, impedance matching and amplification. The drive amplifier is the link between the input source and the ADC.

When selecting an amplifier, ac performance factors such as bandwidth, slew rate, noise and distortion drive the decision-making process with dc errors considered secondarily. One of the difficulties that arises during amplifier selection is that op amps are not normally specified in the same manner as ADCs. ENOB (effective number of bits) is a key ac parameter used for ADCs. It is calculated based on SINAD (signal to noise + distortion) in dB, where

$$\text{ENOB} = \frac{\text{SINAD} - 1.76}{6.02}.$$

By measuring the THD+*N* (total distortion + noise) in dB of the TLV2462 and TLV2772 in different circuit topologies and substituting THD+*N* for SINAD when calculating ENOB, the amplifier's performance is directly comparable to the TLV2544/TLV2548 ADC.

Test circuits

The input to the TLV2544/TLV2548 ADC is modeled as shown in Figure 1. During sampling the input is active and appears as a series resistor and shunt capacitor. Typical values are 1 kΩ and 60 pF. When not sampling, the input impedance of the ADC is high.

Figure 2 shows the non-inverting, inverting and differential amplifier circuits that are tested. A 1-kΩ resistor in series with a 68-pF capacitor is placed on the output of each amplifier to simulate the input of the ADC. The value of resistive components, R, is varied between 1 kΩ,

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Figure 1. Equivalent ADC input

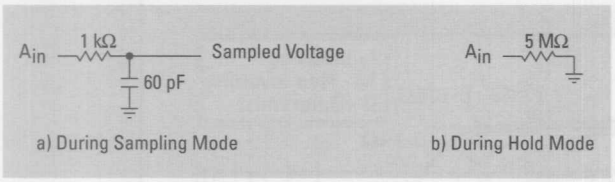
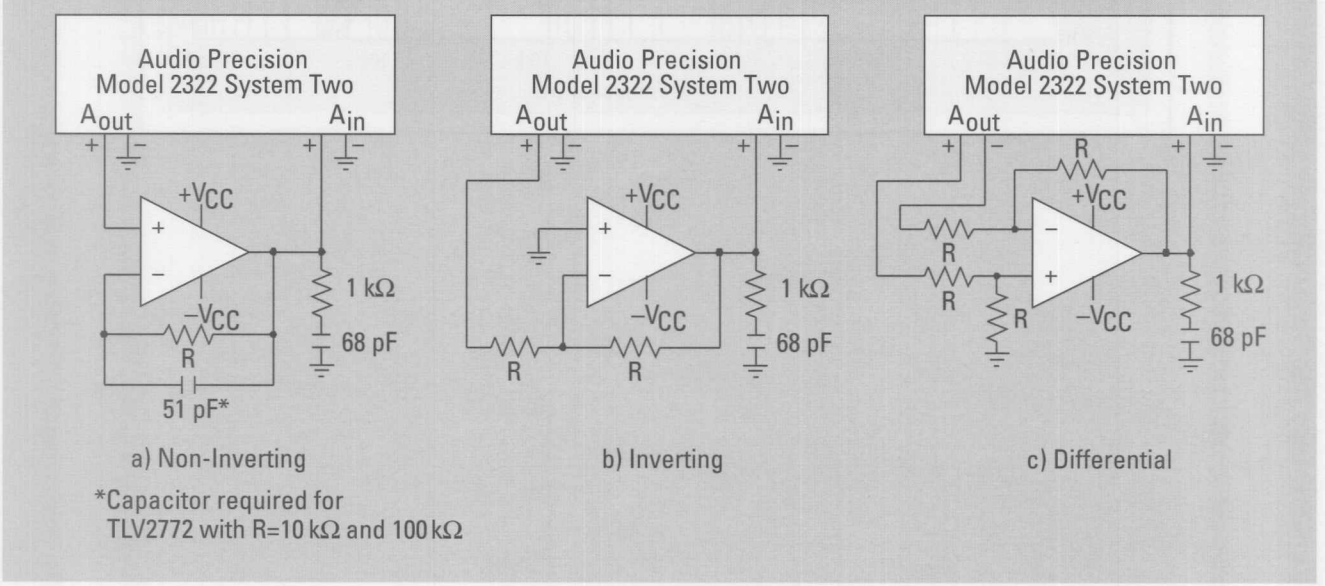


Figure 2. Test circuits



See next two pages for related websites

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10 kΩ and 100 kΩ to measure their effect on the ENOB performance. Note that in the TLV2772 non-inverting circuit with 10-kΩ and 100-kΩ resistor values, a small capacitor is required in the feedback circuit for stability due to the capacitance of the cabling and measuring instrument. Note also that R = 0 Ω is tested for the non-inverting amplifiers. Compare the test results from the TLV2462 in Figures 3 and 4 with the TLV2772 in Figures 5 and 6.

An Audio Precision model 2322 – System Two is used to measure the THD+*N* of the amplifier circuits. The analog test signal is a sine wave that is swept from 10 Hz to 200 kHz. The measurement bandwidth is 10 Hz to 500 kHz.

It is assumed that the amplifier is operated at the same voltage as the ADC—3.3 V or 5 V. Typically, the amplifier is biased so that with zero input the output is at half the full-scale voltage of the ADC. To simplify testing, the amplifiers use supply voltages of ±1.65 V to simulate a 3.3-V system and ±2.5 V to simulate a 5-V system. The input signal is referenced to ground with peak levels of 0.89 V and 1.78 V. These are equivalent to –1-dB levels in 2-V and 4-V full-scale systems.

Test results

Calculating

$$\text{ENOB} = \frac{(\text{THD} + N) - 1.76}{6.02},$$

Figures 3 to 6 show the results of testing the ENOB with the TLV2544/TLV2548 ADC shown for comparison.

Conclusion

The data shows the TLV2462 and TLV2772 inverting and differential amplifier topologies with resistive elements of R=10 kΩ result in the best amplifier performance. This result may appear surprising at first since the noise gain of the inverting amplifier is twice that of the non-inverting amplifier. The larger values of measured THD+*N* in the non-inverting mode stem from the fact that the input bias point is made to move through most of its common mode voltage range resulting in larger distortion products, with noise being less dominant. The input bias point of the differential amplifier is also made to change, but only one quarter as much. In the inverting topology, the input remains biased midway between the power supply rails. This optimizes distortion performance.

Figure 3. The TLV2462 at 3.3 V

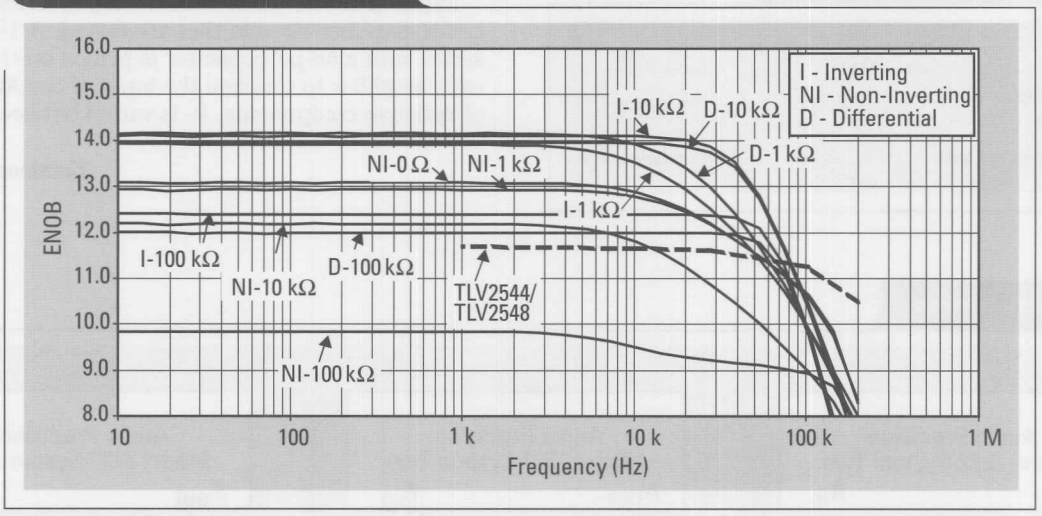


Figure 4. The TLV2462 at 5 V

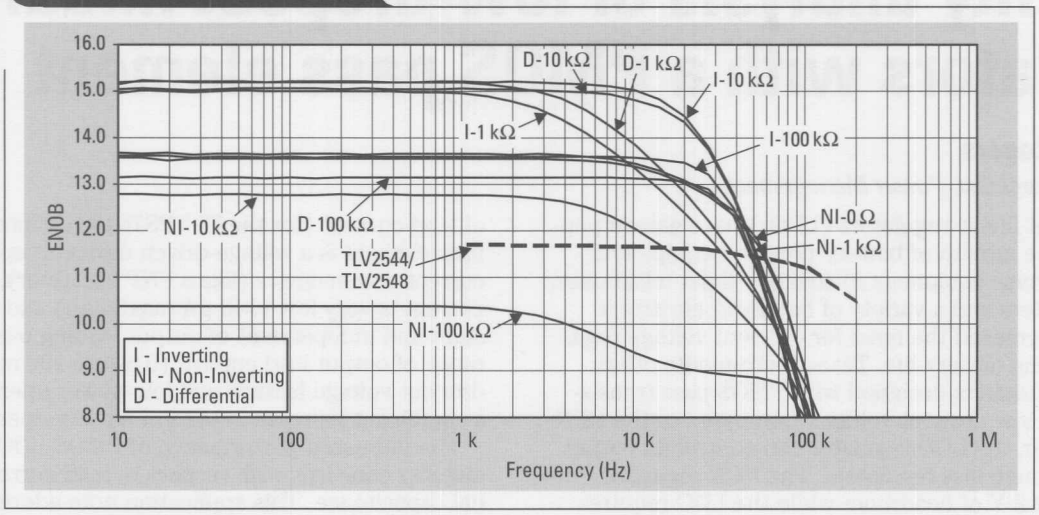


Figure 5. The TLV2772 at 3.3 V

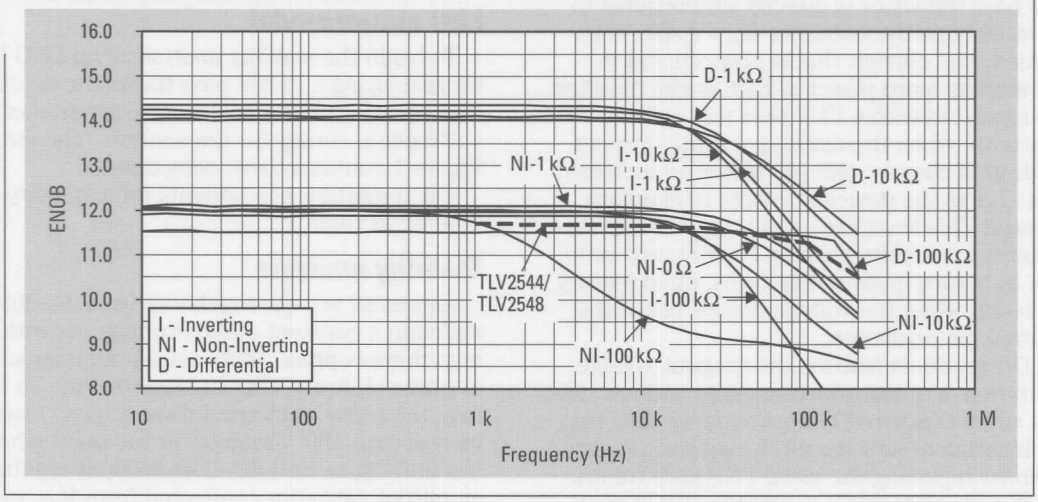
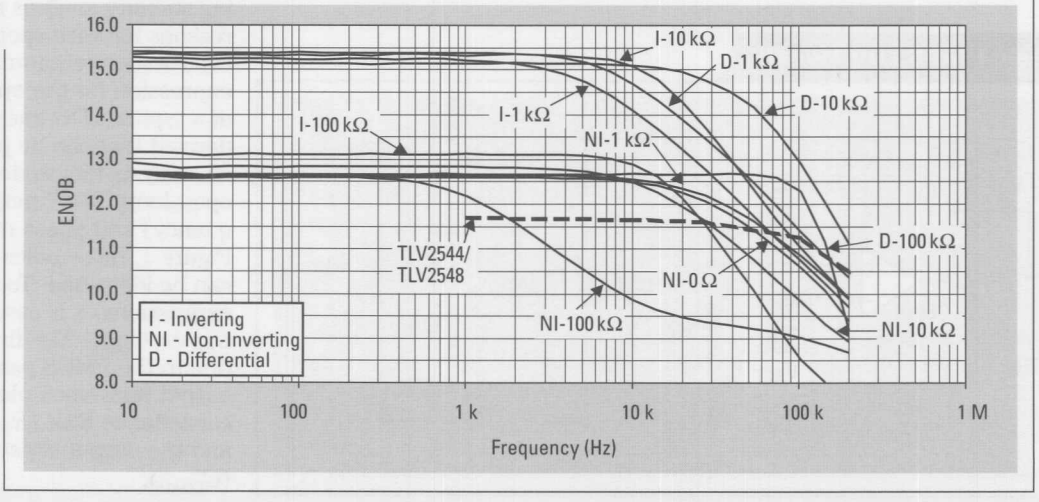


Figure 6. The TLV2772 at 5 V



Stability analysis of low-dropout linear regulators with a PMOS pass element

By Everett Rogers

Application Specialist, Power Management

Low-dropout linear regulators (LDOs) have gained popularity with the growth of battery-powered equipment. Portable electronic equipment including cellular telephones, laptop computers and a variety of handheld electronic devices has increased the need for efficient voltage regulation to prolong battery life. Texas Instruments offers several LDO products designed with PMOS pass transistors with very low dropout voltage. Compared to the NPN linear regulator, the LDO regulator can control its output voltage with much less headroom. The NPN regulator requires about 2 V of headroom while the LDO requires less than half a volt.

Some vendors offer LDO linear regulators designed with PNP pass transistors. For these regulators, the base current for the pass transistor is directly proportional to the load current through the regulator ($I_B = I_C/\beta$). This results in a "quiescent" current that is proportional to load current—wasting more power at high loads. Another disadvantage associated with a PNP pass transistor is its tendency to saturate when the device goes into dropout. The resulting drop in current gain (β) forces an increase in base current (I_B) as the device attempts to maintain the output voltage. This translates into large start-up currents, and systems with limited supply current may even fail to start up. In battery-powered systems, rapid battery discharge can result when the voltage decays below the minimum required for regulation.

TI's PMOS LDO products feature low-dropout voltage, low-power operation, a miniaturized package and low quiescent current when compared to conventional LDO regulators. A combination of new circuit design and process innovation enabled replacing the usual PNP pass transistor with a PMOS pass element. Because the PMOS pass element behaves as a low value resistor near dropout, the dropout voltage is very low—typically 300 mV at 150 mA of load current (for the TI TPS76433). Since the PMOS pass element is a voltage-driven device as opposed to a current-driven device (like a PNP transistor), the quiescent current is very low (140 µA maximum) and remains constant and independent of output loading over the entire range of output load current (0 mA to 150 mA). The low-dropout voltage feature and low-power operation result in a significant increase in system battery operating life.

The increased performance of PMOS LDOs comes with stability concerns with respect to load current and external capacitance. This application note addresses the reasons behind the possibility for an unstable LDO linear regulator. An analysis of the control loop and a discussion of parameters affecting loop stability is presented.

LDO circuit model

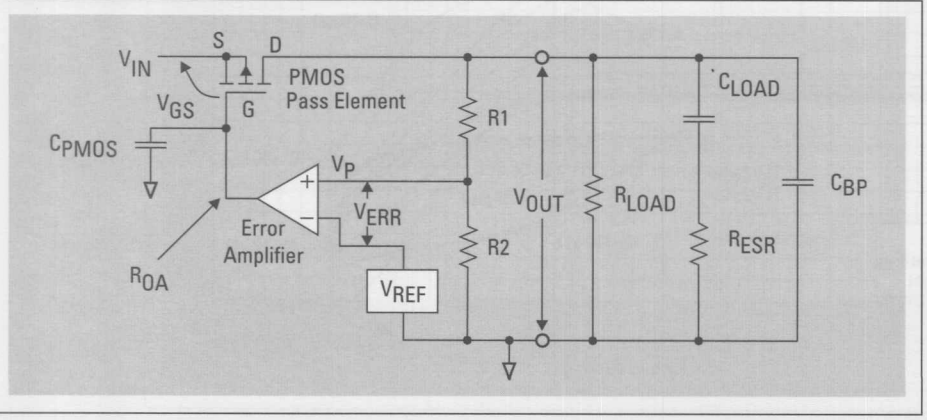
To begin the stability analysis of an LDO linear regulator employing a PMOS pass transistor requires a model that contains all the necessary components to provide sufficient accuracy for the analysis. The circuit shown in Figure 1 contains these components.

The important components for a stability analysis are defined in Table 1.

Stability analysis

Almost all voltage regulators use a feedback loop to maintain a constant output voltage. As with any feedback loop there is phase shift around the loop and the amount of phase shift determines loop stability. To have a stable loop the phase shift around the (open) loop must always be less than 180° (lagging) at the point where the loop has unity gain, or 0 dB. Low-dropout regulators require an output capacitor connected from V_{OUT} to GND to stabilize the internal control loop. Typically, a minimum value of output capacitance is specified. In addition, a range of ESR (equivalent series resistance) is specified. The following stability analysis reveals the reasons for such specific output capacitance requirements. An expression for the open-loop gain of a typical LDO linear regulator is derived that can be plotted using an analysis tool to determine the open-loop UGF (unity gain frequency) and phase margin (ϕ_m). In Figure 1, three poles and one zero can be identified. To simplify the expressions, it is assumed that $C_{BP} << C_{LOAD}$. The first pole ($p1$) is due to the PMOS pass transistor output resistance plus the output capacitance ESR ($R_{O\,PMOS} + R_{ESR}$) and the output capacitance (C_{LOAD}).

Figure 1. Basic PMOS LDO model



$$p1 = \frac{1}{2\pi\,(R_{O\,PMOS} + R_{ESR}) \times C_{LOAD}}$$

The second pole ($p2$) is due to the output capacitance ESR (R_{ESR}) and the estimated bypass capacitance, C_{BP}.

$$p2 = \frac{1}{2\pi \times R_{ESR} \times C_{BP}}$$

The third pole ($p3$) is due to the error amplifier output resistance (R_{OA}) and the equivalent PMOS capacitance (C_{PMOS}).

$$p3 = \frac{1}{2\pi \times R_{OA} \times C_{PMOS}}$$

The single zero ($z1$) is derived from the output capacitance ESR (R_{ESR}) and the output capacitance (C_{LOAD}).

$$z1 = \frac{1}{2\pi \times R_{ESR} \times C_{LOAD}}$$

The remaining information required is the error amplifier gain, feedback network gain and PMOS pass transistor gain. Values given for the following gains are for illustrative purposes and are reasonable values for 100-mA output LDO linear regulators.

The error amplifier gain (G_{EA}) is assumed to be 35 dB.

$$G_{EA} = 35\text{ dB} = 56.2$$

The feedback network gain (G_{FB}) is simply the gain of the resistive divider, R1 and R2. For an output voltage of 3.3 V (for example) and a reference voltage of 1.192 V, the feedback network gain is

$$G_{FB} = \frac{V_{REF}}{V_{OUT}} = \frac{1.192}{3.3} = 0.36 = -8.8\text{ dB}.$$

The PMOS pass transistor gain (G_{PMOS}) is assumed to be 8 V/V.

$$G_{PMOS} = 8 = 18.1\text{ dB}$$

The resulting expression for open-loop gain is

$$G_{OL}(s) = G_{EA} \times G_{FB} \times G_{PMOS} \cdots \times \frac{1 + \frac{s}{2\pi fz1}}{\left(1 + \frac{s}{2\pi fp1}\right) \times \left(1 + \frac{s}{2\pi fp2}\right) \times \left(1 + \frac{s}{2\pi fp3}\right)}.$$

The following component values are used (for illustrative purposes):

$R_{O\,PMOS}$ = 65 Ω
R_{ESR} = 2 Ω
C_{LOAD} = 10 µF
C_{BP} = 0.5 µF
R_{OA} = 300 kΩ
C_{PMOS} = 200 pF

For the given component values, the pole and zero locations are:

$fp1$ = 238 Hz
$fp2$ = 159 kHz
$fp3$ = 2.65 kHz
$fz1$ = 7.96 kHz

The DC gain is G_{OL}(DC) = 162 ⇒ 44.2 dB.

Continued on next page

Table 1. Definition of stability analysis components

Reference voltage	This voltage is the basis for the output voltage. The output voltage cannot be more accurate or stable over temperature than the reference voltage. For many of TI's LDOs, this voltage is 1.192 V.
Error amplifier	The function of the error amplifier is to compare a scaled representation of V_{OUT} to the reference voltage and amplify the difference. The error amplifier output then drives the PMOS pass transistor to adjust V_{OUT}. A typical error amplifier DC gain is 25 dB to 45 dB, depending on the particular LDO.
Feedback network	The feedback network is a resistive voltage divider. This network scales V_{OUT} such that the scaled V_{OUT} is equal to the reference voltage when V_{OUT} is at its nominal value. For fixed output LDOs these resistors are internal to the LDO and have a relatively high value in order to minimize current drain.
R_{LOAD}	Load resistance. $R_{LOAD} = V_{OUT}/I_{OUT}$.
C_{LOAD}	The capacitance placed on the output of the LDO for loop stability that is typically specified to be a minimum of 4.7 µF to 10 µF. Depending on the type of capacitor, it may have an internal ESR ranging from 10 Ω to 10 mΩ.
R_{ESR}	The equivalent series resistance of the output capacitor. Depending on the particular output capacitor, this resistance may include an external resistance placed in series with the output capacitor. This resistance is sometimes called the *compensation series resistance*.
C_{BP}	An estimate of the bypass capacitors placed across the power supply leads of the ICs powered by the LDO. These capacitors are usually 0.1-µF ceramics and have very low ESR.
C_{PMOS}	The capacitance connected to the output of the error amplifier. This capacitance is due mainly to the capacitance of the PMOS pass element and is usually in the range of 100 pF to 300 pF.
R_{OA}	The equivalent output resistance of the error amplifier. This parameter is one of the few parameters the LDO designer can choose to insure stability. A typical design value is approximately 300 kΩ.
PMOS pass	The series pass element in the LDO. This transistor operates as a variable resistance connected between the input and the output. The resistance is controlled by the gate-to-source voltage. The output resistance, $R_{O\,PMOS}$ (different from R_{OA}), is used in the stability analysis.

Figure 2 shows a gain-phase plot of the above equation using the values given. Also shown in the plot are the pole and zero frequencies. Figure 2 shows a stable system. The UGF is approximately 14 kHz with a phase margin of 66°. Notice that the single zero occurs at a lower frequency than the UGF. This configuration of two poles and one zero below the UGF produces a stable system.

To illustrate the need for a minimum value of R_{ESR}, the gain-phase plot is recalculated with R_{ESR} set to 10 mΩ. Figure 3 is a gain-phase plot of the same system, except with R_{ESR} = 10 mΩ. The UGF is now 10 kHz with an unacceptable phase margin of 16°. With a very low ESR value such as this, pole *p2* and zero *z1* are both at frequencies much higher than the UGF. This leaves two poles below the UGF, producing an unstable system.

To illustrate the need for a minimum value of C_{LOAD}, the gain-phase plot is recalculated with C_{LOAD} set to 1.0 µF.

Figure 2. LDO open-loop response (stable)

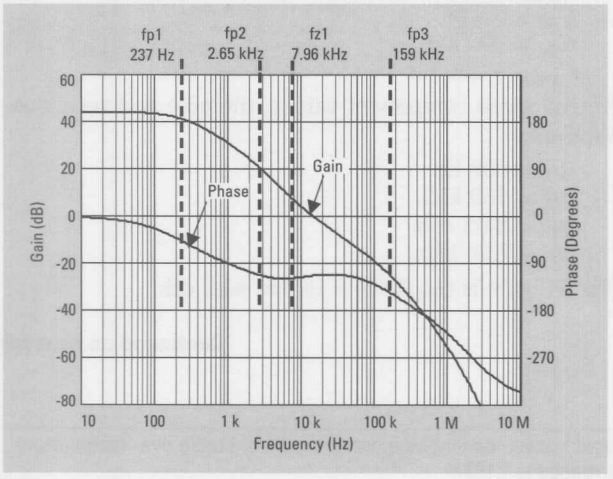


Figure 3. LDO open-loop response (unstable). R_{ESR} = 10 mΩ.

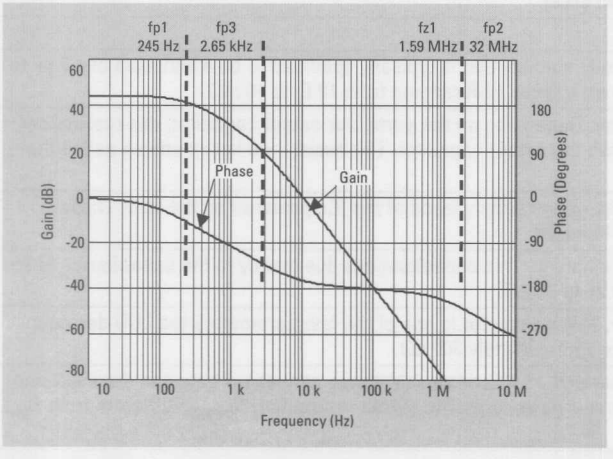


Figure 4. LDO open-loop response (unstable). C_{LOAD} = 1 µF.

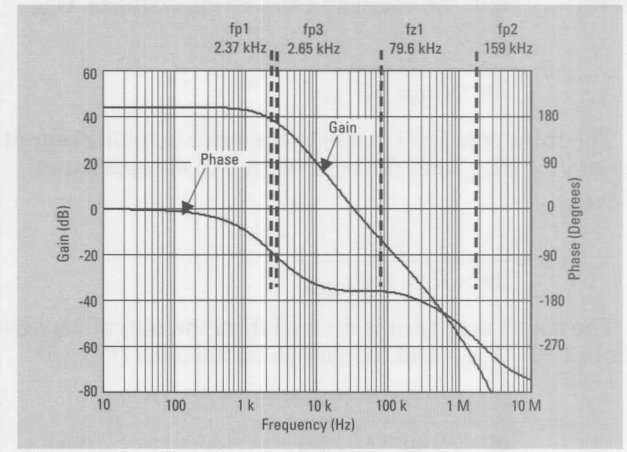


Figure 4 is a gain-phase plot of the same system, except with C_{LOAD} = 1.0 µF. The UGF is now 32.4 kHz with an unacceptable phase margin of 18°. With a low C_{LOAD} value such as this, pole *p2* and zero *z1* are both at frequencies higher than the UGF. This leaves two poles below the UGF, producing an unstable system.

Summary

Low-dropout linear regulators with a PMOS pass element give increased performance over linear regulators employing NPN or PNP pass elements. With this gain in performance comes a concern over control loop stability. This is common to all LDO designs, especially ones using PMOS or PNP pass elements. Selecting the appropriate output capacitor and resistor to place in series with the capacitor easily solves most stability issues. The expression for the (open) control loop gain and phase vs. frequency is derived and an illustrative example is given. The expression for the control loop shows what parameters and/or component values affect stability.

References

1. M. Kay, "Design and Analysis of an LDO Voltage Regulator with a PMOS Power Device," preliminary paper pending publication, Texas Instruments Inc., Dallas.
2. T. Kugelstadt, "Fundamental Theory of PMOS Low-Dropout Linear Regulators," Application Report, Texas Instruments Inc., literature number SLVA068.
3. G. A. Rincon-Mora and P. E. Allen, "Optimized Frequency-Shaping Circuit Topologies for LDOs," *IEEE Transactions on Circuits and Systems – II: Analog and Digital Signal Processing*, Vol. 45 (June 1998), pp. 703-708.

(0 V to 3.5 V) using the TI TPS5210

By Bang Sup Lee
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This application note describes the design of a 12-V input/0-V to 1.3-V output synchronous buck regulator using the TI TPS5210 programmable controller. Although the output voltage can be extended down to 0 V to 1.3 V using the auxiliary circuitry described in this note, the supply will still be capable of providing an output voltage range from 1.3 V to 3.5 V, determined by the voltage identification code (VID).

The TPS5210, a synchronous buck regulator controller, provides an accurate, programmable supply voltage suitable for microprocessor power applications that require fast response to rapidly changing loads and precise voltage regulation.

A simplified diagram of the regulator circuit is shown in Figure 1. The diagram shows the 1% voltage reference, hysteresis control and gate drivers with adaptive deadtime control. The reference voltage ranging from 1.3 V to 3.5 V is determined by the VID. The hysteresis controller senses the output voltage through the feedback loop (V_{SENSE} pin) and the supply regulates the DC voltage level to the reference value (V_{REF}) set using the data on the VID pins. When the feedback voltage V_{SENSE} is rescaled to a specific value, the regulator output voltage can be extended to 0 V to 1.3 V.

Figure 2 shows the application circuit of the extended 1-V output, which is identical to the application shown in Figure 1 (TPS5210 data sheet, literature number SLVS171A, Figure 18), except for the auxiliary circuit.

Figure 1. Synchronous buck regulator using the TPS5210

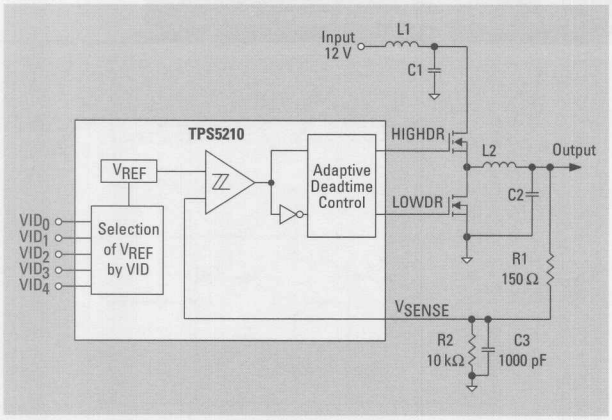
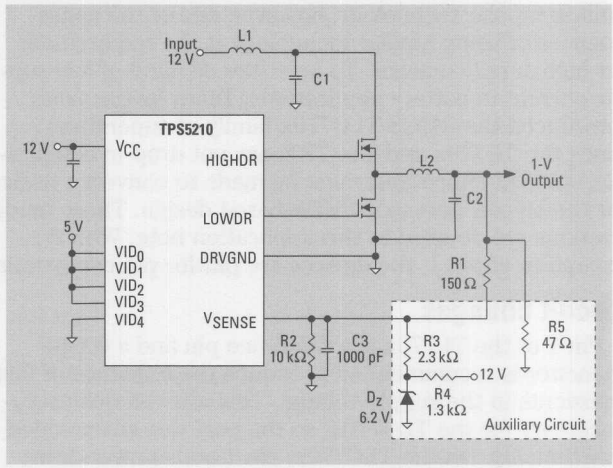


Figure 2. 1-V regulator using the TPS5210



Adding a few inexpensive components in the feedback path of TPS5210 enables the generation of 0-V to 1.3-V regulated.

To operate the circuit for a 1-V output, the voltage reference (V_{REF}) should be set to 1.3 V using the VID code. The internal hysteresis comparator in the TPS5210 regulates the output voltage to 1.3 V, comparing V_{REF} (1.3 V) with the output feedback voltage, V_{SENSE}. Since the output voltage feedback signal (V_{SENSE}) is scaled to 1.3/1.0 V (V_{SENSE}/V_{OUT}) by using a resistive voltage divider (R1-R3) as shown in Figure 2, the output voltage is regulated at 1 V. The demand resistor (R3) value required for a 1-V output is calculated using Equation 1.

$$R3 = \frac{V_{DZ} - V_{SENSE}}{\frac{V_{SENSE} - V_{OUT}}{R1} + \frac{V_{SENSE}}{R2}} = \frac{6.2 - 1.3}{\frac{1.3 - 1.0}{150} + \frac{1.3}{10k}}$$

$$= 2.3\ k\Omega \qquad (1)$$

This method can also be applied to any output voltage ranging between 0 V to 1.3 V by using the above equation.

Migrating from the TI TL770x to the TI TLC770x

By Benjie Balser
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Device functionality

The TI TL770x is a proven processor supervisory circuit built in bipolar technology, however, one of the consequences of using bipolar technology is the requirement for high supply current. To meet the demand of low supply current in battery applications, Texas Instruments introduced the CMOS TLC770x family of supervisors. Since the TL770x and TLC770x are not drop-in compatible, some modifications must be made to convert a design for the bipolar part to a CMOS-based design. Those modifications are detailed in this application note. With the exception of pin 1, the devices are pin-for-pin compatible.

Circuit changes

Pin 1 of the TL770x is a reference pin and a 0.1-µF capacitor is recommended to reduce the influence of fast transients in the supply voltage. This was not deemed necessary for the TLC770x, so the part was given added functionality. On the TLC770x, pin 1 adds power-down support for static RAM. When the TLC770x's pin 1 (CONTROL) is left floating (there is an internal pull-down resistor), RESET will act as active high. The voltage monitor contains additional logic intended for control of static memories with battery backup during power failure. Figure 2 shows the configuration for driving the chip select (/CS) of the memory circuit with the RESET output of the TLC770x while the CONTROL input is driven by the microprocessor's memory bank select signal (/CSH1). The memory circuit is automatically disabled during a power loss. In most applications, this function is not needed and leaving the pin floating retains the part's normal functionality.

Timing

The delay timing of the two parts is also different due to their internal current sources. Figure 3 shows the timing equations used to determine the time delay (t_d) for the A and B version of the bipolar TL770x and for the TLC770x CMOS device.

Another difference between the TL770x and TLC770x is the requirement for pull-up and pull-down resistors on the TLC770x reset outputs; the TLC770x does not have this requirement. The bipolar device uses open collector outputs and the CMOS device has push-pull outputs (see Figure 4).

Finally, the internal reference voltage is different for the two devices. The reference voltage on the bipolar part is 2.5 V, whereas the reference voltage for the CMOS part is 1.1 V. This will only affect the design of the adjustable part when selecting the resistor divider values between the supply and sense lines.

Figure 1. Different functionality of pin 1

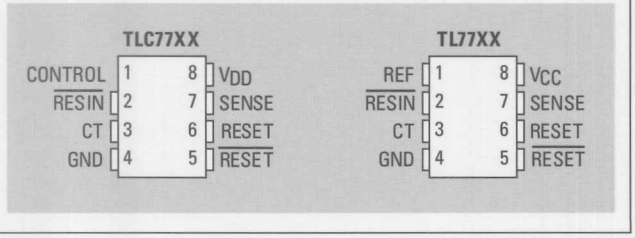


Figure 2. Data retention during power-down

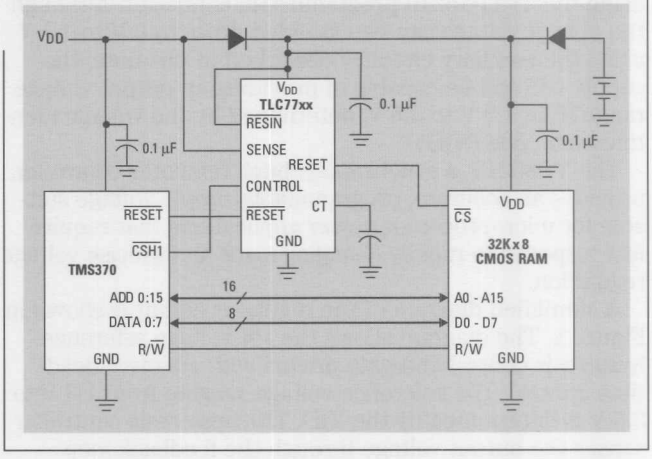
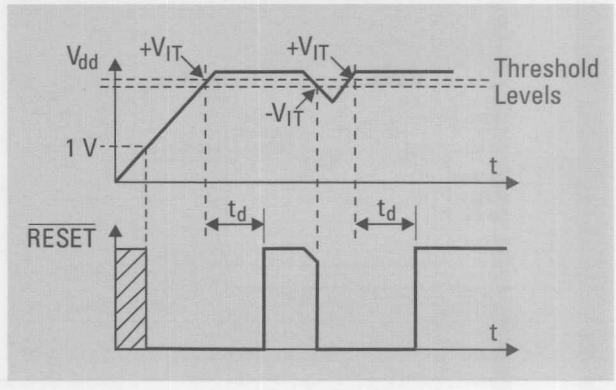


Figure 3. Definition of delay time, t_d



TL770xA: $t_d = 1.3 \times 10E4 \times C_T$ **(1)**
TL770xB: $t_d = 2.6 \times 10E4 \times C_T$ **(2)**
TLC770x: $t_d = 2.1 \times 10E4 \times C_T$ **(3)**

where t_d = delay time in seconds and C_T = capacitance in farads.

Figures 5 and 6 show a comparison of the functional block diagrams of both circuits.

Summary

To convert a design from the bipolar TL770x to the CMOS TLC770x, the following circuit changes must be made:

1. Remove the capacitor on pin 1.
2. Change the value of the timing capacitor according to the timing equations.
3. Remove the pull-up and pull-down resistors on the reset outputs.
4. Recalculate the resistor divider based on the different reference voltage (only necessary for the adjustable part).

Figure 4. Totem-pole vs. open collector outputs

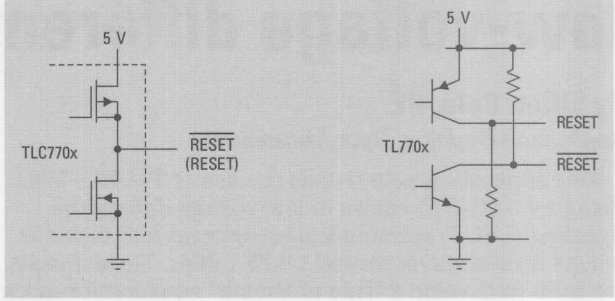


Figure 5. Internal functional diagram of the CMOS TLC770xx

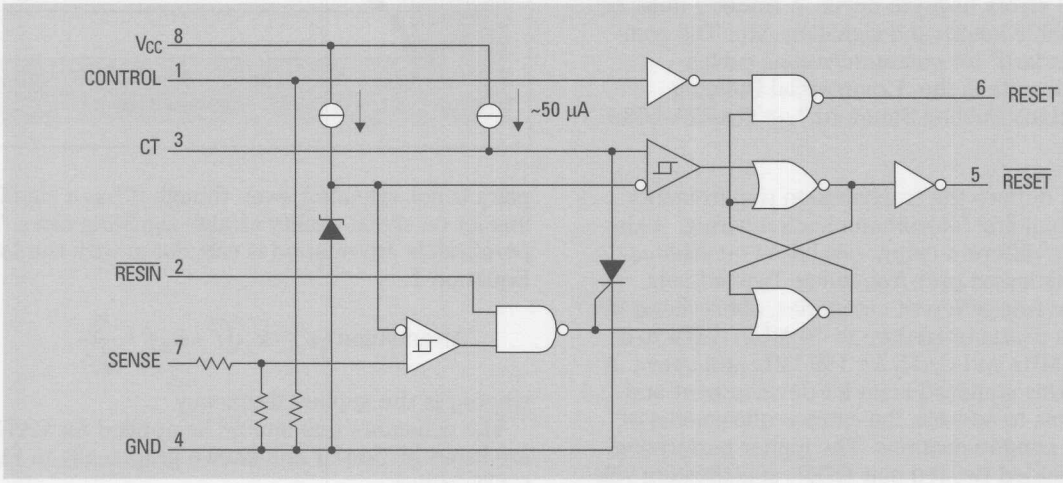
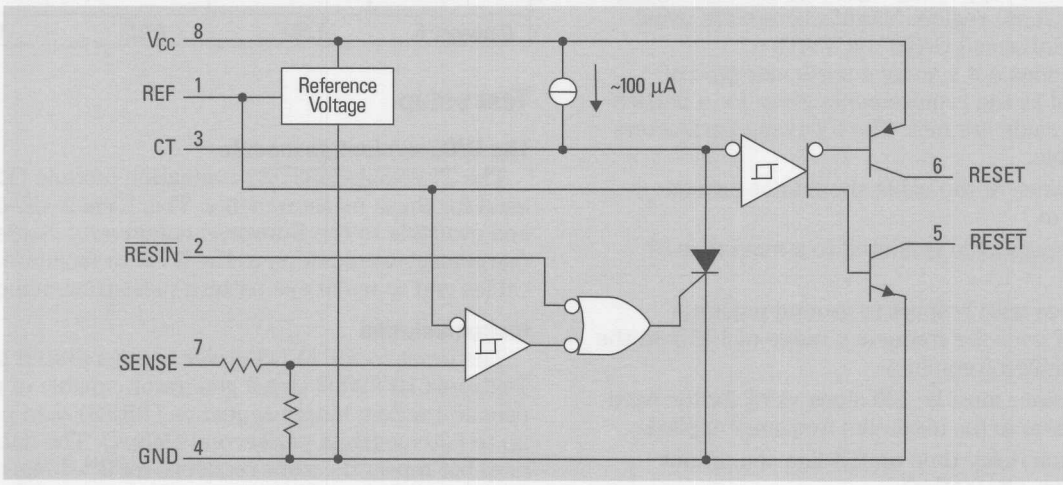


Figure 6. Internal functional diagram of the bipolar TL770xx



TIA/EIA-568A Category 5 cables in low-voltage differential signaling (LVDS)

By Elliott Cole, P.E.
Application Engineer, Data Transmission

This application note details the use of TIA/EIA-568A Category 5 (CAT5) cables in low-voltage differential signaling (LVDS) communication systems and includes results from tests on several CAT5 cables. These results are used to develop a "rule-of-thumb" equation for quickly estimating the distance and signaling rate that can be achieved with LVDS devices and CAT5 cables. When it comes to LVDS interfaces, designers want to send data very quickly. Unfortunately, at high data rates (>100 Mbps) the characteristics of the cable degrade the signal quality to a point where errors begin to occur. A tradeoff must be made between cable length and signaling rate. The commonly used "standard" for communications cables referred to in this note is the "Commercial Building Telecommunications Cabling Standard," or TIA/EIA-568A.

TIA/EIA-568A

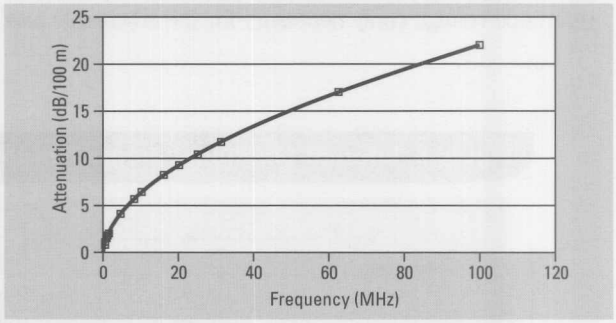
TIA/EIA-568A defines the transmission requirements for commercial building telecommunication wiring. It classifies cabling into different categories based on attenuation and crosstalk losses over frequency. Twisted-pair cable is classified into different categories, abbreviated by "CATX." CAT3 is characterized up to 16 MHz, CAT4 to a maximum of 20 MHz and CAT5 for 100 MHz and above. A new revision of this standard is under development and will add categories to address the cable requirements of high-speed data communications. The higher performing cables of this shielded twisted pair (STP) specification will be called CAT7, while the unshielded twisted-pair (UTP) cables (with lower performance) will be classified as CAT6. So far, there is no "official" CAT designation, however, some manufacturers have announced availability of products capable of supporting signaling rates in the gigabit-per-second (Gbps) region. Manufacturers are using terms such as "Enhanced CAT5" or "CAT5+."

The standard does not specify a particular type of shielding, as long as the requirements given for a particular class of UTP cable are met. The following parameters are for CAT5 cable:

- The DC resistance of the cable should not exceed 9.38 ohm/100 m.
- The mutual capacitance is limited to a maximum of 5.6 nF/100 m.
- The capacitance with respect to ground must not exceed 330 pF over the frequency range of 1 kHz to the maximum specified frequency.
- The line impedance must be 100 ohms +15% for the bandwidth of 1 MHz up to the maximum frequency applied.
- The propagation delay time on the line should not exceed 5.7 ns/m (@10 MHz).

It is important to point out that the skew (created by the difference in lengths between two conductors of a pair) is not specified, even though it has a significant impact on signal quality at high signaling rates. The permissible attenuation is calculated with the formula in Equation 1.

Figure 1. Permissible attenuation on a CAT5 cable



$$\text{Attenuation}(f) = k_1\sqrt{f} + k_2 f + \frac{k_3}{\sqrt{f}} \quad (1)$$

where f is the applied frequency.

The constants that should be applied for CAT5 cables are listed in Table 1 and shown graphically in Figure 1 for CAT5 cables.

Table 1. Attenuation constants

	$k_1(\sqrt{s})$	$k_2(s)$	$k_3\left(\frac{1}{\sqrt{s}}\right)$
Category 5	1.967	0.023	0.050

Test setup

The LVDS evaluation module

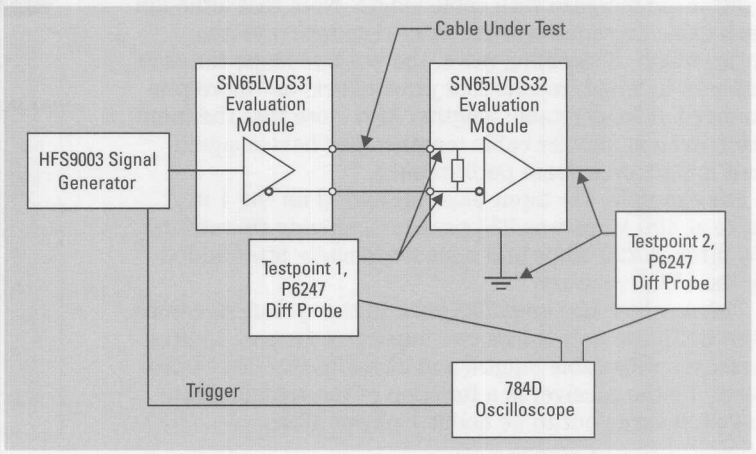
The TI SN65LVDS31/32 evaluation module (EVM) was used for these measurements. This EVM is CE-certified and available to the European community. Solder posts (terminals) were added to the EVM to facilitate changing cables and to make eye pattern measurements quickly.

Instrumentation

The input to the LVDS driver was generated by a Tektronix HFS9003 signal generator capable of generating pseudo-random binary sequence (PRBS) data patterns at up to 630 megabits per second (Mbps). The data pattern does not repeat the same sequence for 2^{16}–1 bits or 64 kbits. The input levels to the LVDS31 driver were set to 0 V (low) and 2.7 V (high) and the transition rate (rise and fall times) set to 800 ps.

and Tektronix P6247 differential probes were used. Both the scope and probe have a bandwidth of 1 GHz and a capacitive load of less than 1 pF. For signals in the range of 400 Mbps and above, an even higher bandwidth is recommended. (As a rule of thumb, the fifth harmonic—i.e., 2 GHz—should be detected.) The basic test setup is shown in Figure 2.

Figure 2. Test setup



Measurements

Measurements were performed on seven CAT5 cables while varying the signaling rate and cable length. For each PRBS data measurement, non-return to zero (NRZ) formatted signals were used. The experiments were conducted in a laboratory standard environment at room temperature in an area where a considerable amount of electronic equipment was in operation. The PRBS patterns were applied and the eye pattern recorded at the end of the cable (i.e., the input of the receiver) and at the output of the receiver. Tests were carried out on each cable using eye patterns to measure the peak-to-peak jitter. System level jitter should be a function of both signaling rate and cable length. This was tested by using CAT5 cable lengths of 1 m to 20 m at signaling rates of 50 Mbps to 450 Mbps in 50-Mbps increments.

Jitter measurement

The eye pattern is a useful tool for measuring the overall signal quality at the end of a transmission line. It shows all of the effects of systemic and random distortion and shows the time during which the signal may be considered valid. A typical eye pattern is illustrated in Figure 3 with the significant attributes identified.

Several characteristics of the eye pattern indicate the signal quality of the transmission circuit. The height or "opening" of the eye above or below the receiver threshold level at the sampling instant is the noise margin of the system. The spread of the transitions across the receiver thresholds measures the peak-to-peak jitter of the data signal. The signal rise and fall times can be measured relative to the 0% and 100% levels provided by long series of low and high levels.

Jitter occurs in the time frame during which logic state transition of the signal occurs. The extreme values are caused by long sequences of one logic state preceding a transition. The jitter may be stated as an absolute number or as a percentage with reference to the unit interval. The unit interval (UI) or "bit length" equals the reciprocal value of the signaling rate. The width is the UI—i.e., the time during which the logic state "could" be valid. Percent jitter is commonly expressed as the jitter time divided by the UI (times 100) and represents the time during which the logic state should be considered invalid.

Results

As expected, system jitter is a function of both cable length and signaling rate. The first set of measurements taken determined the extent which these two parameters effected system level jitter. Jitter was recorded at the input and output of the LVDS32 receiver with different test cables. The jitter results for each cable type and length were averaged for each specific signaling rate.The average input jitter measurements are shown in Figure 4.

Continued on next page

Figure 3. Typical eye pattern

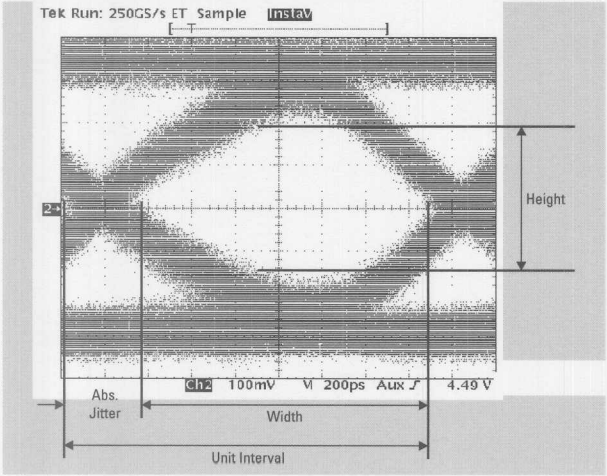
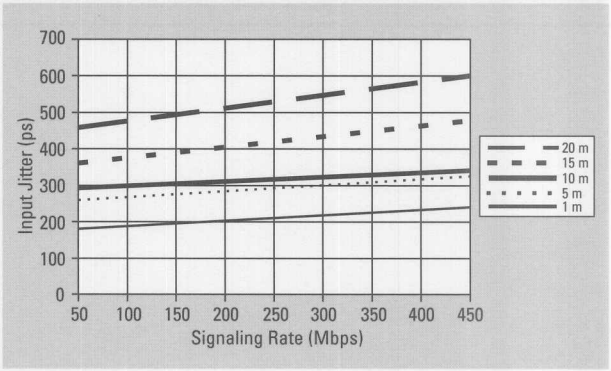


Figure 4. Input jitter vs. signaling rate for CAT5 cables



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Jitter did increase with cable length. Note that although each cable provided a linear jitter response over the entire range of signaling rates, the positive slope for each increase in length means that jitter effects are more pronounced at longer cable lengths. Also, note that the input jitter, even at shorter cable lengths, may have a significant impact on system performance.

For example, the input jitter measured on the 1-m cable at 400 Mbps was 225 ps, which already represents 5% jitter at 220 Mbps and does not include jitter added by the LVDS receiver.

The receiver also amplifies jitter in the system as can be seen in Figure 5. It shows two important factors: 1) jitter increases with cable length, and 2) additional jitter introduced by the receiver is a function of the signaling rate. In fact, it turns out to be about 1 ps per Mbps.

The "rule of thumb"

Based on the information contained in Figures 4 and 5, system (cable plus receiver) jitter can be estimated closely as a function of both cable length and signaling rate. Equation 2 has been developed from the data in Figure 4 and 5 to approximate the jitter out of an LVDS receiver given a specific length of CAT5 cable and signaling rate. Since it is an average, based upon several CAT5 cables, it is fair to assume that better cables will yield better results. Notice that it is based on cable lengths of 1 m to 20 m and signaling rates of 100 Mbps up to 400 Mbps. No assumptions should be made about performance of either the cable or LVDS receiver outside these bounds.

Figure 5. Jitter increases through a receiver

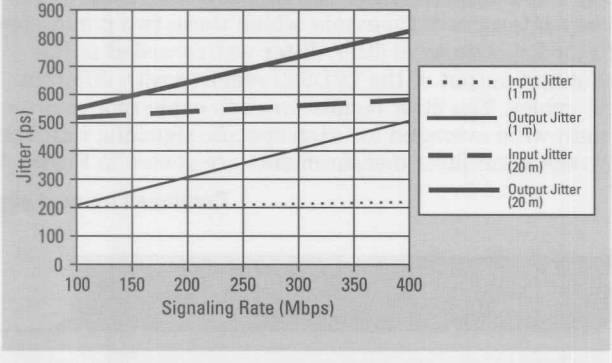
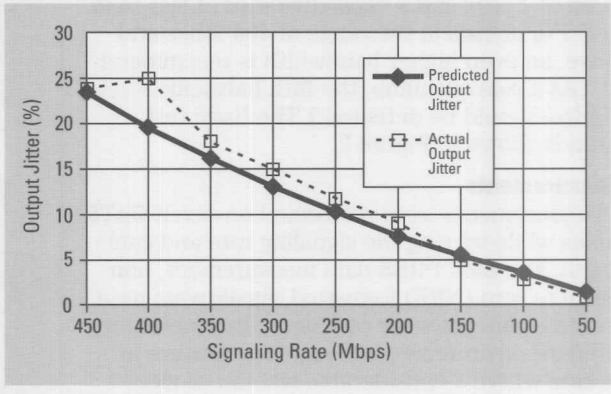


Figure 6. Actual vs. predicted jitter (5-m CAT5 cable)



$$\text{Output jitter} = \frac{\left\{1+\left[\frac{0.0023\times S.R.}{1+\frac{(C.L.-1)}{7.63}}\right]\right\}\times\{[200+(15\times C.L.)]\times S.R.\}}{10{,}000} \quad (2)$$

where $S.R.$ is the signaling rate in Mbps and $C.L.$ is the cable length in meters.

The "rule of thumb" was tested against one of the cables selected at random. The actual jitter performance versus the "rule of thumb" predicted jitter performance with a 5-m cable is shown in Figure 6.

Conclusion

As expected, the "rule-of-thumb" equation works better at the lower signaling/data rates. Less jitter was apparent from the cable and the LVDS receiver at low signaling rates where CAT5 cables are specified. It's important to realize that all of the cables tested were developed before the LVDS standard was released. It's fair to assume that none of these CAT5 cables were developed to support signaling/data rates of 400 Mbps.

Reducing the output filter of a Class-D amplifier

By Mike Score
System Specialist, Audio

A properly designed Class-D output filter limits supply current, minimizes EMI and protects the loudspeaker from switching waveforms. However, it also significantly increases the total design cost. The current recommended second-order output filter for the TI TPA005D02 is 30% of the audio power amplifier (APA) solution cost. This application note details the second-order Butterworth filter and two reduced filtering techniques, each providing a different price/performance node. The first alternative to the Butterworth filter reduces the output filter by half and the second option completely eliminates the filter. The filters were tested using Texas Instruments TPA005D02 Class-D APA. Design decisions based on the measured results and conclusions are drawn to provide practical solutions for applications with different price/performance nodes.

Second-order Butterworth low-pass filter

The second-order Butterworth low-pass filter is the most common filter used in Class-D amplifier applications. This filter uses two inductors and three capacitors for a bridged-tied-load (BTL) output, which can be seen in Figure 1. The primary purpose of this filter is to act as an inductor at the switching frequency. The inductor is needed to keep the output current constant while the voltage is switching. If the outputs do not see an inductive load at the switching frequency, the supply current will increase until the device is unstable. Higher inductance at the output yields lower quiescent current (supply current with no input) because it limits the amount of output ripple current. The filter protects the speaker by attenuating the switching frequency. The inductors, L1 and L2, and the capacitor C1 form a differential filter that has an attenuation slope of 40 dB per decade. The majority of the switching current flows through C1, leaving very little current to be dissipated in the speaker. The filter also reduces EMI. The previously described differential filter reduces differential radiation. Inductors L1 and L2 and capacitors C2 and C3 form common-mode filters that further reduce EMI. See the "TPA005D02 Class-D Stereo Audio Power Amplifier Evaluation Module User's Guide"[1] for details on how the output filter was designed.

Figure 1. Full second-order Butterworth filter

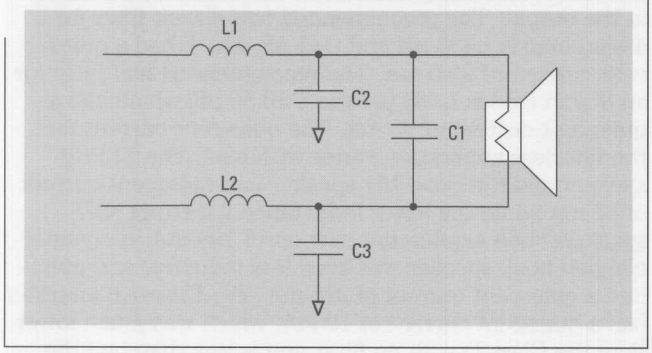
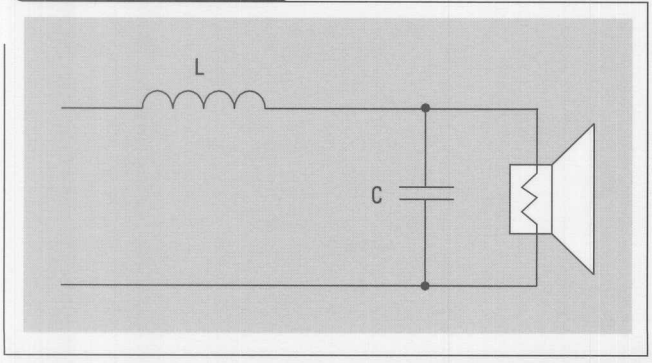


Figure 2. Half filter



Half filter

The half filter (shown in Figure 2) eliminates one of the inductors and the two capacitors to ground. The other inductor must be doubled (for half filter C = C1 of the full filter) to obtain the correct cut-off frequency. This filter is still inductive at the switching frequency because capacitor C looks like a short at the switching frequency and each amplifier output sees inductor L. The supply current is even lower for this application because the total inductance stays the same as the full filter but the DC resistance (DCR) from the inductors is reduced causing less power loss in the filter. The speaker is still protected in this application although one of the speaker terminals is directly tied to the switching waveform. The differential signal is still filtered and the audio output rides on the switching waveform. Although this filter attenuates the differential signal, which reduces EMI, it does not attenuate the common mode signal, which could cause EMI problems. Methods to reduce EMI will be discussed in a later section.

No filter

The filter can be eliminated if the speaker is inductive at the switching frequency. How is it possible to eliminate the filter and place a pulse-width modulated (PWM) square wave directly across the speaker? The PWM waveform is the sum of the switching waveform and the input audio signal with gain. The human ear acts as a band-pass filter, hearing only the frequencies between approximately 20 Hz and 20 kHz. The switching frequency is much greater than 20 kHz, so the only signal heard is the input

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audio signal with gain. The main drawback to not using a filter is that the switching waveform is dissipated in the speaker, which leads to a higher quiescent current, $I_{DD(q)}$. This is because the speaker is both resistive and reactive, where an LC filter is almost purely reactive. A more inductive speaker yields lower quiescent current, so it is better to use a two or more layer voice coil speaker for a high inductance in this application. A concern with the switching waveform being dissipated in the speaker is that it may cause damage to the speaker. A primary concern is speaker wear due to a rail-to-rail square wave driving the speaker whenever the amplifier is on. For a 250-kHz switching frequency, this is not an issue because the speaker cone movement is proportional to $1/f^2$ for frequencies beyond the audio band, thus the amount of cone movement at the switching frequency is insignificant.[2] Damage could occur to the speaker if the voice coil is not designed for the added power. The added power to the load is less than the added power taken from the supply because the device cannot have efficiency greater than 100%. The added power can be calculated using Equation 1, where P_{SW} is the added power dissipated in the speaker, $I_{DD(q)(\text{with speaker load})}$ is the quiescent current measured with speaker load, $I_{DD(q)(\text{no load or filter})}$ is the quiescent current measured with no load, V_{DD} is the supply voltage and N is the number of channels.

(1)

$$P_{SW} < \frac{(I_{DD(q)(\text{with speaker load})} - I_{DD(q)(\text{no load or filter})})V_{DD}}{N}$$

The added power from the switching waveform can be calculated. A supply current of 83-mA was measured with the TPA005D02 EVM connected to the speakers available with the TI Plug-n-Play base kit. The supply current with no load was measured at 23 mA. A 5-V supply was used and, because TPA005D02 is a stereo device, N=2; therefore, the maximum added switching power dissipated in the speaker is 150 mW. Originally, 3-watt speakers were required. The filterless solution requires 3.15-watt speakers. Another concern is that not filtering causes the amplifier to radiate EMI along the lines from the amplifier to the speaker. The filterless application is not recommended for EMI-sensitive circuits.

Measured results

The quiescent current, total harmonic distortion plus noise (THD+N) and intermodulation distortion (IMD) were measured for the full-, half- and no-filter applications. Each measurement was done using a TPA005D02 Class-D 2-W amplifier. A measurement was made in each case with the TI TPA0102 used for comparison. The measurement set-up and results will be discussed for each test.

Table 1. Quiescent current for various filter applications using the TPA005D02 and the TPA0102

APPLICATION	LOAD	L (µH)	$I_{DD(q)}$ (mA)
Full filter	Any size resistor or speaker load	15	39
Half filter L = DS3316-P-xxx	Any size resistor or speaker load	15	42
		22	35
		33	29.5
		47	27
Half filter L = DS5022-P-xxx	Any size resistor or speaker load	68	25
		100	24
		150	23
No filter	Notebook speaker		215
	NXT speaker		199
	TI PnP speaker		83
	Bose 151 speaker		83
TPA0102	Any load		19

Quiescent current

The quiescent current for the full-, half- and no-filter applications is tabulated in Table 1. The quiescent current of the full- and half-filter applications was independent of the load and varied greatly with inductor value, but the no-filter application's quiescent current was dependent on the inductance of the speaker. The full-filter quiescent current was measured using the filter designed for a 4-ohm load, where L1=L2=15 µH, C2=C3=0.22 µF, and C1=1 µF, with the components labeled as shown in Figure 1. The quiescent current of the half-filter application shown in Figure 2 was measured with C = 1 µF, and L was varied to show how increasing inductance decreases ripple current at the output. The recommended half-circuit filter for a 4-ohm load is L=33 µH and C=1 µF, which had a quiescent current of 29.5 mA. The recommended half filter for an 8-ohm load is L=68 µH and C=0.56 µF, which had a quiescent current of 25 mA. The quiescent current for the filterless application varies with load. The TI PnP speaker and the Bose 151 speaker had quiescent current of 83 mA while the lower inductance flat panel NXT speakers[3] had a quiescent current of 199 mA. A commercial notebook speaker was even less inductive and exhibited a quiescent current of 215 mA. The Class-AB amplifier had a quiescent current of 19 mA, which was much lower than the Class-D with no filter and is less than half the Class-D with full filter, but not much lower than the Class-D with half filter.

Total harmonic distortion plus noise (THD+*N*) was measured with the Audio Precision II analyzer. In each measurement, an RC filter with a cut-off frequency of 37 kHz was added between the output to ground to filter the common-mode signal into the Audio Precision. The bandwidth of the Audio Precision was set from 10 Hz to 22 kHz and an internal 20-kHz low-pass filter was also used to ensure that the switching frequency did not influence the THD+*N* measurement. Band-limiting the measurement ensured that only the audible harmonic distortion and noise were measured. The amplifiers were set at a gain of 22.5 V/V. THD+*N* versus output voltage at 1 kHz was measured with the TPA005D02 with full, half and no filter. The same test was performed using the TPA0102.

filter applications had approximately the same THD+*N* across all power levels. The Class-D without the output filter actually had lower THD+*N* at the lower power levels than the TPA005D02 with the filter and the TPA0102. The TPA0102 had approximately the same THD+*N* as the TPA005D02 with the full and half filters at low to mid powers, and lower THD+*N* at the higher powers.

IMD

Intermodulation distortion (IMD) occurs when two or more signals are input into an amplifier and the sum and difference of the input frequencies are present at the output. IMD is a good measurement of linearity (the lower the IMD, the more linear the device under test). IMD is

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Figure 3. THD+*N* vs. V_{out}

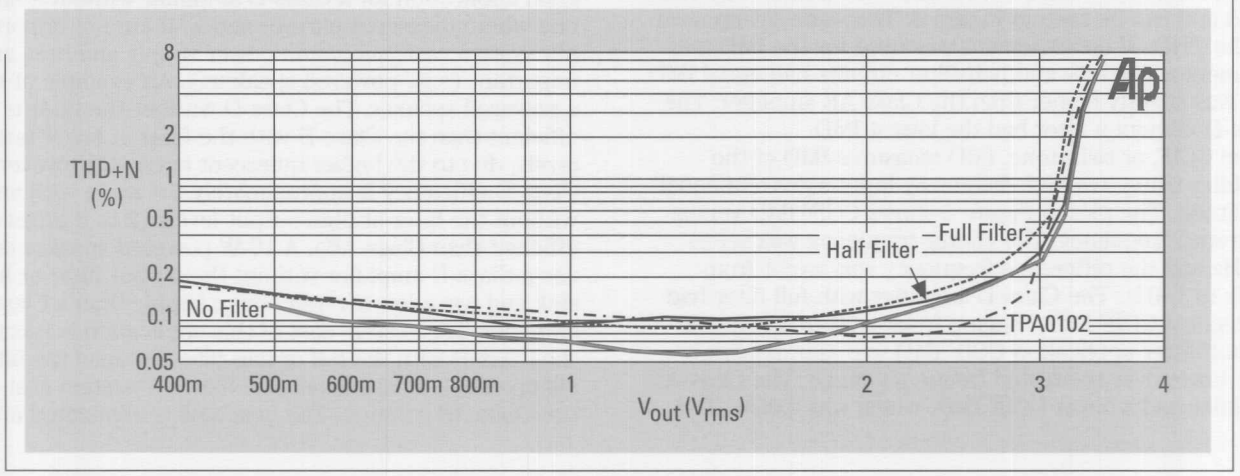
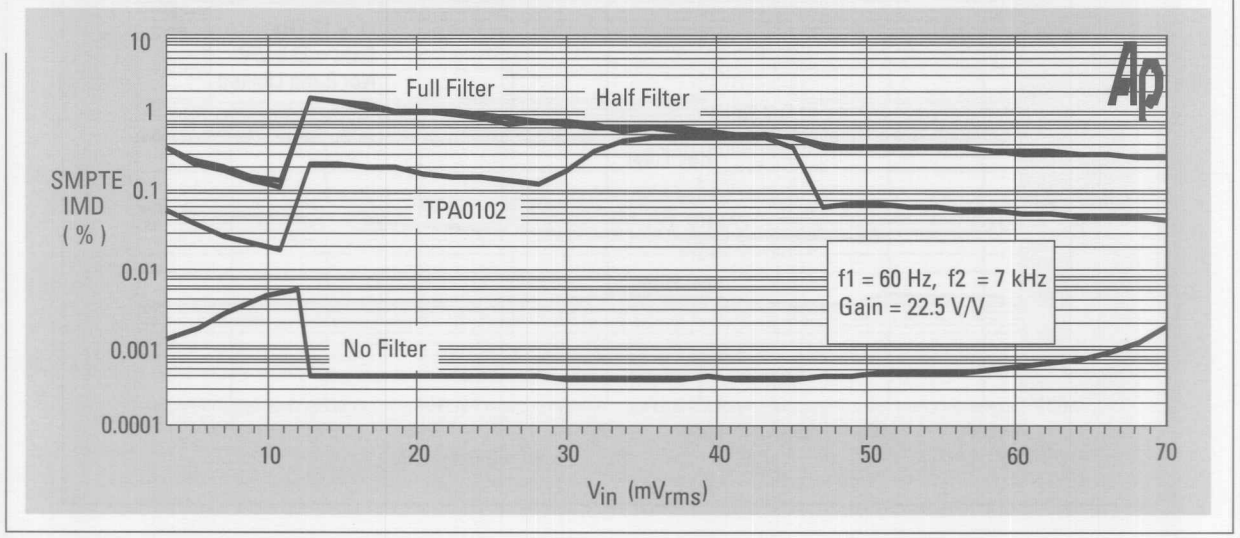


Figure 4. SMPTE IMD vs. input voltage



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the ratio of magnitude of the sum and difference signals to the original input signal.

$$IMD = [(V_{f2-f1} + V_{f2+f1})^2 + (V_{f2-2f1} + V_{f2+2f1})^2 + (V_{f2-3f1} + V_{f2+3f1})^2 \ldots]^{0.5}/V_{f2} \quad (2)$$

where V_{f2} is the voltage at the input frequency $f2$, V_{f2+f1} is the voltage at the sum of input frequencies $f1$ and $f2$, V_{f2-2f1} is the voltage at the difference of input frequencies $f1$ and $2*f2$, etc.

The Society of Motion Picture and Television Engineers (SMPTE) standard IMD test is the most common IMD measurement. The SMPTE IMD test inputs a low-frequency 60-Hz and high-frequency 7-kHz sine wave into the device. The low-frequency sine wave has four times the amplitude of the high-frequency sine wave.[4] The SMPTE IMD versus input voltage of the Class-AB and Class-D amplifier with the full, half and no filter was measured and can be seen in Figure 4. The same set-up used for the THD+*N* measurement was used for the IMD measurements. The full- and half-filter circuits had equal IMD that was slightly higher than the Class-AB amplifier. The Class-D without a filter had the lowest IMD.

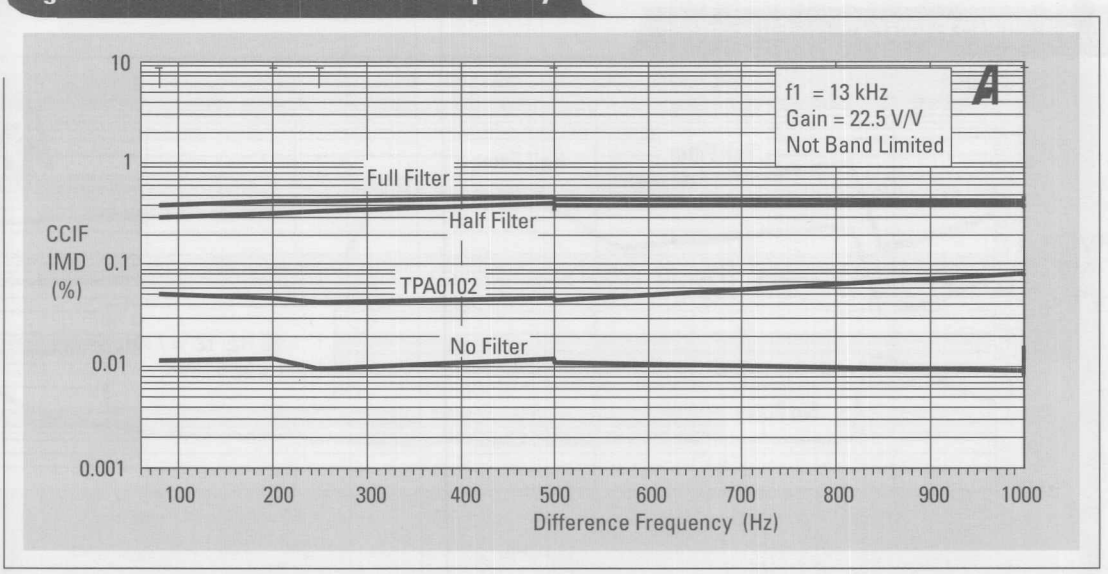
The CCIF, or twin-tone, IMD measures IMD of the amplifier using two high-frequency input signals of equal amplitude. The plot in Figure 5 shows CCIF IMD versus difference frequency. The center frequency was set to 13 kHz and the difference frequency was swept from 80 Hz to 1 kHz. The Class-D amplifier with full filter had the highest CCIF IMD, ranging from 0.4% to 0.5%, and the half-filter application CCIF IMD was approximately 0.1% lower over the tested frequency range. The Class-AB amplifier had a lower CCIF IMD, which was 0.05%. The Class-D without an output filter had the lowest CCIF IMD, which was 0.01%.

Design decisions based on results

Class-D without output filter

The Class-D without the output filter not only had lower THD+*N* and IMD than the Class-D with the filter, it also outperformed the Class-AB device. The two disadvantages of using the Class-D amplifier without the output filter are high quiescent current and high EMI. Quiescent current can be lowered using a speaker with a high inductance, but it is doubtful whether it could ever be lower than an application with a filter. EMI can be lowered using ferrite beads at the output of the amplifier, shielded speakers and shielded speaker wires running to the speakers. EMI can also be reduced by making the distance from the amplifier to the speaker as short as possible and by keeping the positive and negative output wires very close together to reduce common-mode radiation. A good application for a Class-D amplifier without a filter is one where quiescent current and EMI are not important, but system cost, maximum power supply and heat are important (e.g., powered speakers). An example of this is a powered speaker. The Class-D without the filter is less efficient than the Class-D with the filter at lower output levels, due to the higher quiescent current. However, the Class-D efficiency is approximately the same with and without the filter at high output levels (2 to 3 times more efficient than Class-AB). A 10-W powered speaker could use a Class-D amplifier without the output filter or heat sink and use a lower-rated power supply than a Class-AB amplifier. The system cost of this application is less than the Class-D with the full or half filter because the filter is eliminated, and less expensive than the system cost of the Class-AB solution. The heat sink is eliminated and the

Figure 5. CCIF IMD vs. difference frequency



power supply is reduced in a 10-W Class-D filterless application, but the Class-D amplifier is slightly more expensive than an equivalent Class-AB amplifier. The speaker inductance must be high, and the amplifier must be close to the speaker in this application.

Class-D with half filter

Class-D with a half filter had a lower quiescent current and performed as good as or better than the Class-D with full filter in THD+*N* and IMD. The quiescent current lowers as the inductor of the half filter increases. As inductance increases, peaking occurs at the corner frequency of the filter. The corner frequency can be set outside the audio band so the peaking has no effect on sound quality. Peaking occurs regardless of LC design with a speaker load when designing for a resistive load. The half filter designed for a 4-ohm resistive load uses a 33-µH inductor with a 1-µF capacitor, and the half filter designed for an 8-ohm resistive load uses a 68-µH inductor and a 0.56-µF capacitor. Each of these examples exhibits peaking at the corner frequency because the speaker is not purely resistive at the corner frequency. An RC network can be used across the load to reduce reactance of the load to limit peaking. If quiescent current is very important, the designer can increase L and lower C, decreasing the quiescent current and keeping the corner frequency in place. The designer should design the filter with the speaker load to ensure the corner frequency peaking is outside the audio band. The only disadvantage with the half-filter application is that it has higher common-mode EMI than the full filter due to the filter not having a common-mode filter. The common-mode EMI should not be a problem in most systems if the positive and negative output signal paths are very close together to cancel common-mode radiation. The filter should be as close to the amplifier as possible to reduce EMI. EMI can be further reduced with ferrite beads, shielded speaker wire and using good board layout. The Class-D with half filter is an ideal circuit where battery life, heat and system cost are primary issues. The Class-D with half filter is the most efficient circuit at low and high powers and has a lower cost than the Class-D with full filter. These issues make the half filter Class-D the ideal circuit for notebook PCs. Notebook PCs are very concerned with battery life and heat, while system costs are still important. EMI issues are well understood by notebook designers, so the additional EMI generated by the half-filter implementation should not be a problem.

Class-D with full filter

Class-D with full filter had lower IMD than the Class-D without a filter and higher quiescent current than Class-D with a half filter. It also has a higher system cost than either circuit. Designers should use Class-D with the full output filter when heat, battery life and EMI are concerns. An example of this would be a boom-box, where the amplifier is in the same location as an AM receiver, where the switching frequency is close to the band of frequencies that the AM receiver is demodulating. Another example would be any device that has wires connecting the amplifier to the speakers. The wires act as an antenna, and if not filtered, the switching frequency could radiate to other devices in the vicinity.

Conclusion

It is possible to reduce the output filter in certain applications. This application note has shown that reducing the output filter does not mean reduction in quality. The Class-D amplifier with and without the output filter had approximately the same THD+*N*. The Class-D amplifier actually had lower IMD without the output filter. The quiescent current of the Class-D amplifier was lower using the half filter than the full filter, making the Class-D amplifier even more efficient. The designer who is primarily concerned with maximum heat and power-supply constraints and is not concerned with EMI and quiescent current could use the Class-D amplifier without a filter to save cost. A designer who is primarily concerned with heat and battery life and has EMI as a secondary concern could use a Class-D amplifier with a half filter. Applications that are very EMI-sensitive and/or have devices operating around the switching frequency of the Class-D amplifier should use a full filter.

References

1. "TPA005D02 Class-D Stereo Audio Power Amplifier Evaluation Module User's Guide," Texas Instruments Inc., September 1998, literature number SLOU032.
2. Martin Colloms, *High-Performance Loudspeakers* (London: Pentech Press Limited, 1985), pp. 18-26.
3. http://www.nxtsound.com
4. Bob Metzler, *Audio Measurement Handbook* (Audio Precision, Inc., 1993), pp. 37-39; http://www.ti.com/sc/apa

Power supply decoupling and audio signal filtering for the Class-D audio power amplifier

By Richard Palmer
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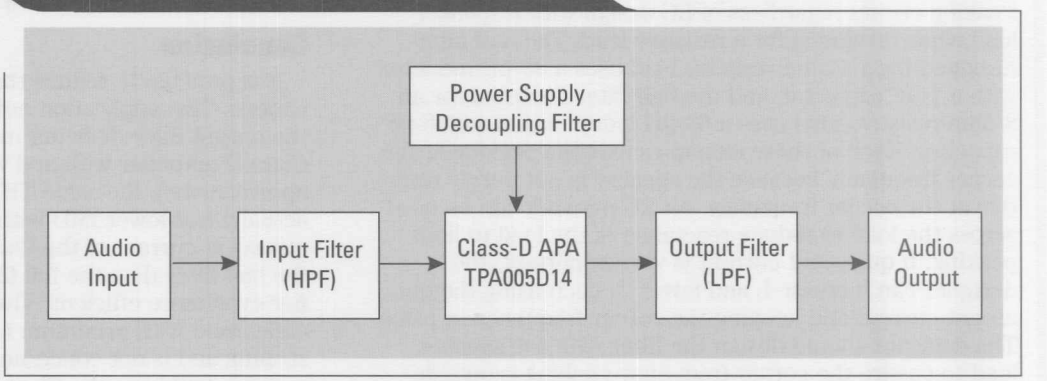
Introduction

Class-D audio amplifiers are very similar to switch-mode power supplies in that both compare an input signal with a reference to create an error voltage that controls a pulse-width modulation (PWM) circuit. The PWM signal controls the switching action of the output power stage consisting of DMOS power transistors in an H-bridge configuration. The result is a square wave output which, when passed through a low-pass filter (LPF), produces an amplified version of the audio input. The Texas Instruments website has information available on the operation of the Class-D audio power amplifiers.[1]

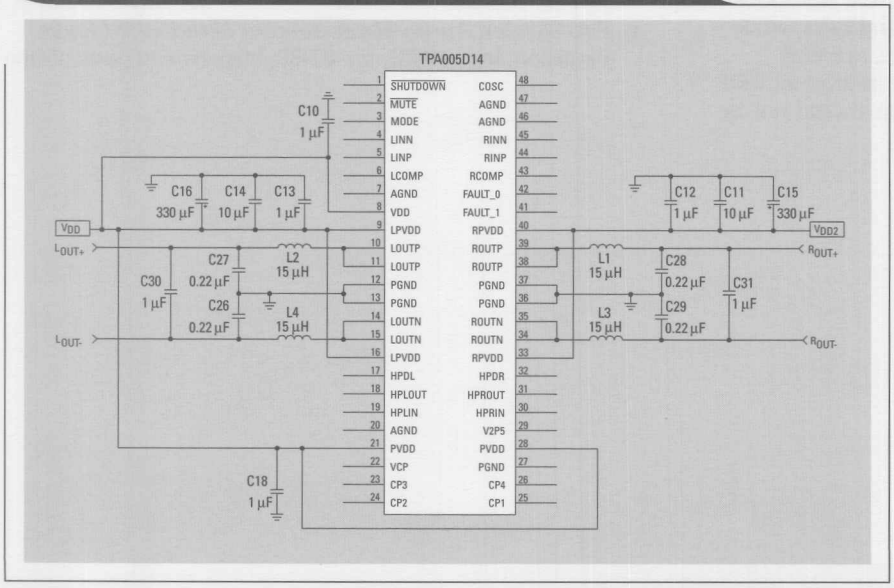
This application note describes proper decoupling of the power supply, selection and implementation of audio input and output filters, and some basic layout considerations for the TI TPA005D14 Class-D stereo audio power amplifier. Figure 1 shows the major function blocks that support the Class-D amplifier in the audio system. Each of the filter functions will be explained with emphasis on selection and placement of components.

Figure 1. Simplified Class-D system overview



A partial schematic of the TPA005D14 EVM, SLOP 204, is shown in Figure 2. The 5-V device is capable of delivering 2 watts of continuous output power into a 4-Ω load with less than 0.5% total harmonic distortion across the 20-Hz to 20-kHz audio frequency range. The full EVM schematic and performance characteristics can be found in the user's guide.

Figure 2. Power supply decoupling capacitor circuit



Power supply decoupling[2]

Power supply decoupling requires providing the bulk capacitance needed to supply the low-frequency charge and the capacitance needed for the switching transient response.

Bulk capacitance

Power supply decoupling plays a key role in achieving top performance from Class-D amplifiers. The capacitance at the power inputs provides a low-impedance voltage source for the device that reduces the ripple of the power supply voltage created by the pulse currents of the Class-D device. This reduces the distortion in the output and produces a much cleaner audio output. Capacitors are modeled using equivalent series resistance (ESR), equivalent series inductance (ESL), capacitive reactance (X_C) and inductive reactance (X_L). The equivalent impedance of a

Equation 1.

$$Z = \sqrt{\text{ESR}^2 + (X_C - X_L)^2} \quad (1)$$

X_L is small for frequencies below 1 MHz and can be neglected since the switching frequency range of the TPA005D14 is 100 to 500 kHz. X_C is maximum and dominates at DC, and decreases as the frequency increases until resonance is reached ($X_C = X_L$), at which point Z = ESR. The ESR of a capacitor is considered to be constant over the 100-kHz to 500-kHz switching frequency range of the Class-D amplifier. Capacitors C15 and C16 in Figure 2 provide the bulk capacitance required for each channel. Assuming that the power supply current is constant and has negligible ripple, the capacitor current is negligible, and the switching frequency and dc load resistance are known, the peak power for a given load is used to calculate the peak current as shown in Equation 2.

$$I_{\text{Peak}} = \sqrt{P_{\text{Peak}}/R_L} \quad (2)$$

The minimum capacitance, shown in Equation 3, needed to maintain a specified ripple voltage, assuming ESR = 0, is then:

$$C \geq (I_{\text{Peak}} \times T_D \times D_{\text{Max}})/V_{\text{Ripple}} \quad (3)$$

where $T_D = 1/f_{\text{switch}}$ is the period, D_{Max} is the maximum duty cycle and V_{Ripple} is the desired ripple voltage. In almost every case the ripple voltage caused by the ESR will dominate. The ESR required to achieve the same V_{Ripple} for the I_{Peak} from Equation 2 is:

$$\text{ESR} \leq V_{\text{Ripple}}/I_{\text{Peak}} \quad (4)$$

This value assumes that the capacitor ripple is ≤10% of the ESR ripple (the capacitance is ≥10 × C of Equation 3). The capacitor ESR should be 30 to 50% lower than Equation 4 to allow for increases due to temperature, ESL and aging. Capacitors can be paralleled to reduce ESR and power dissipation.

Transient response of the decoupling capacitors

The bulk capacitor C15 (or C16) of Figure 2 is large and requires an electrolytic capacitor. The time required to transfer the charge of C15 to the load is long due to the time constant created between the capacitance and can deteriorate the output signal and cause distortion. The solution is to add two ceramic capacitors to the filter, one immediately adjacent to the power supply pin (C12 and C13 in Figure 2), and the other between the pin and the bulk electrolytic capacitor (C11 and C14 in Figure 2). Capacitor C12 (or C13) is chosen to be very small to provide a short time constant and, consequently, the available charge is small and is quickly depleted by a large current transient. As charge is depleted from C12, charge from C11 (or C14) begins to arrive at the power pin. The charge from C15 then arrives as the charge for C11 is being depleted. The result is a smooth output signal. The voltage on the power pin will drop if the time constant of C11 or C15 is too long. The long time constant of C15 ensures that plenty of charge will be available for the power pin during the remainder of the transient.

Filtering in the audio signal path

Each channel consists of differential amplifier inputs and bridge-tied load (BTL) outputs. Filtering of the inputs is required to avoid DC offsets. The output filter is recommended for applications requiring minimization of quiescent current and EMI. Figure 3 shows the filtering scheme used in the TPA005D14 EVM.

Input filter

The differential input requires filters for both the noninverting and the inverting inputs of the amplifier. The input filters set the low frequency corner and block DC voltages and currents. Each filter consists of one external capacitor (C_{IN}) in series with the fixed internal resistance (R_{IN}) of the amplifier input. This creates a first-order high-pass filter (HPF) with a –3-dB corner frequency shown in Equation 5 of:

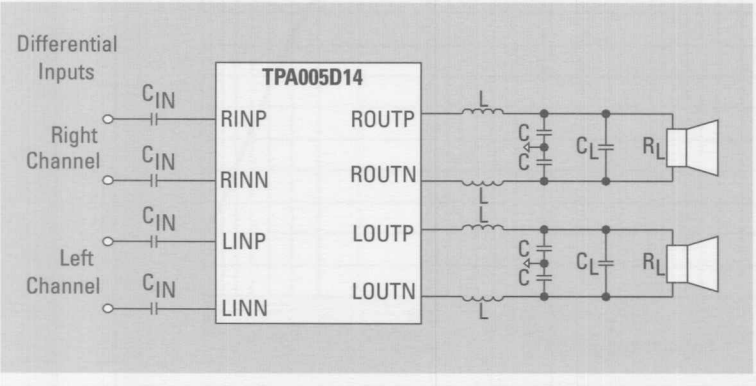
$$f_{\text{LO}} = 1/(2\pi R_{\text{IN}} C_{\text{IN}}) \quad (5)$$

where R_{IN} = 10 kΩ (typical), and C_{IN} = 1 µF for a –3-dB value of 15.9 Hz. f_{LO} can be easily adjusted by changing C_{IN}. The inverting input should be AC grounded for single-ended inputs using the same value of C_{IN} as the noninverting input.

Output filter

Several choices of filters exist and are characterized by the cutoff frequency (–3-dB point), passband gain and ripple, and stop band attenuation. In this case an L-C filter with a Butterworth approximation was chosen for its maximally flat magnitude response and the small number of components required to implement the filter. The order of the filter determines how many poles exist at the same frequency. Each pole increases the attenuation above the cutoff frequency (in the stop band) by 20 dB per decade. A second-order LPF reduces f_s by –40 dB per decade (a 5-V signal will be reduced to 50 mV). The switching frequency (f_s) impacts the choice of the filter order—the higher the f_s, the lower the order required to achieve a given attenuation. The trade-off is a decrease in efficiency and increases in EMI.

Figure 3. Audio signal input and output filters



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The transfer function and –3-dB cutoff frequency are derived in Equation 6 using a half-circuit model and found to be

$$H(s)=\frac{1}{s^2+\sqrt{2}s+1}\times\frac{V_O(s)}{V_I(s)}$$
$$=\frac{1/(2LC_L)}{s^2+\left[1/(R_LC_L)\right]s+\left[1/(2LC_L)\right]} \quad (6)$$

$$f_C=\frac{1}{2\pi\sqrt{2LC_L}} \quad (7)$$

where R_L is the DC resistance of the speaker. The factor of $2L$ is due to the conversion from the half circuit to BTL values. Frequency scaling $\omega_0 = 2\pi f_C$ gives the final Equations 8 and 9 for determining C_L and L. Table 1 shows various values for L and C_L for a given f_C and R_L.

$$C_L=\frac{1}{\sqrt{2}\times R_L\omega_0}=\frac{1}{2\sqrt{2}\times\pi R_L f_C} \quad (8)$$

Table 1. Second-order Butterworth L-C_L values

DC LOAD RESISTANCE, R_L (Ω)	CUTOFF FREQUENCY, f_C (kHz)	INDUCTOR VALUE, L (µH)	CAPACITOR VALUE, C_L (µF)
4	20	22.5	1.41
4	25	18.0	1.13
4	30	15	0.94
4	35	12.9	0.80
8	20	45	0.70
8	25	36	0.56
8	30	30	0.47
8	35	26	0.40

$$L=\frac{\sqrt{2}\times R_L}{\omega_0}=\frac{\sqrt{2}\times R_L}{4\pi f_C} \quad (9)$$

Figure 4 shows the measured response of the TPA005D14 EVM for R = 4 Ω and f_C = 30 kHz using an Audio Precision System II. The response shows a gain of 10 V/V, input corner frequency of 15.9 Hz and an output cutoff frequency of 28 kHz.

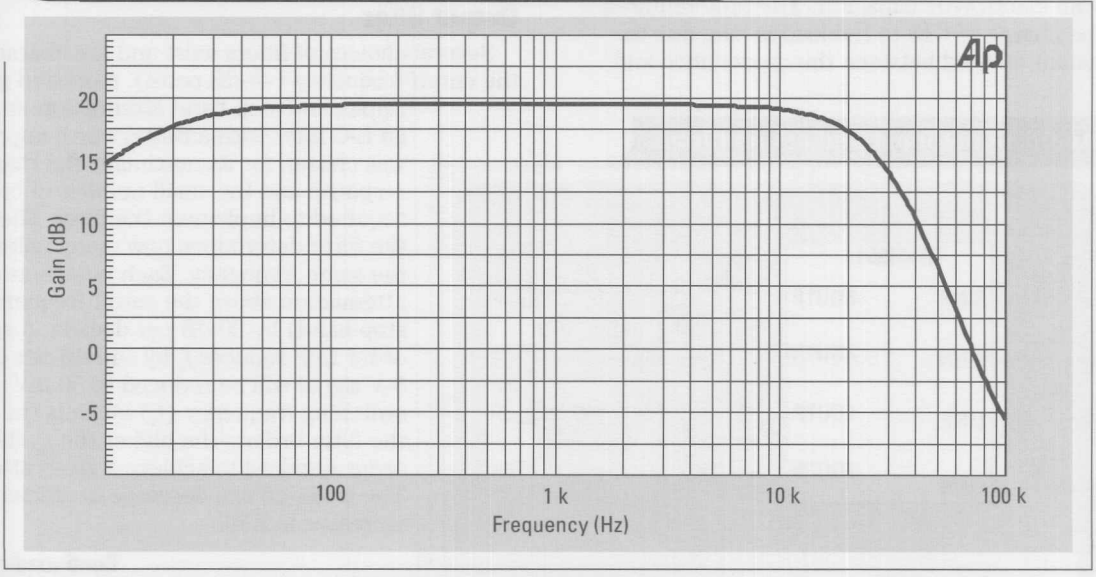
Component selection

The output inductors are key elements in the performance of the Class-D audio power amplifier system. The most important specifications for the inductors are the DC and peak current ratings. These must be chosen to avoid magnetic saturation of the inductor. Magnetic saturation greatly increases distortion in the circuit as the power is increased and can be minimized by choosing an inductor with a current rating greater than the sum of the DC and AC current components. Shielded inductors will also help reduce distortion and EMI and minimize cross-talk. The output filter capacitors, C, in Figure 3 provide high-frequency paths for the switching frequency and noise and assist in supplying charge to the load. Capacitors with a low equivalent series resistance (ESR) and stability over the required voltage and temperature are recommended. These capacitors are empirically chosen to be approximately 20% of C_L.

Layout considerations

Good layout practices and a well thought-out design are critical toward obtaining maximum performance levels from the TPA005D14 amplifier. The main areas of concern are the ground plane, power plane and the audio input and output. Each is discussed briefly below. Refer to Figure 2 for pin numbers and names. See the Class-D application notes and user guides at the Texas Instruments website[1] for more information on the Class-D APA.

Figure 4. Measured response of the TPA005D14 EVM



Ground plane

Experimentation with several types of ground planes has shown that with good planning and layout practices a solid ground plane works as well as other types of grounding schemes. This is due in part to the system's relatively low frequencies of operation and to the careful layout of the components and traces. The solid ground plane also serves to assist the PowerPAD™ [3] in the dissipation of heat, keeping the amplifier relatively cool and eliminating the need for an external heat sink. The pinout of the TPA005D14 allows good separation of the inputs and outputs, minimizing ground return paths and high frequency loops. It is important that any components connecting an IC pin to the ground plane be connected to the nearest ground for that particular pin. Table 2 lists the ground pins for the main sections of the Class-D audio power amplifier. Care should be taken to prevent the ground return path of any high current components (e.g. the output filter capacitors) from directly passing through other ground connections of the IC, particularly the input.

Table 2. Ground pins

GROUND PIN	APPLICABLE CIRCUITS	RELATED IC PINS
47	Controls (shutdown, mute, mode)	1, 2, 3
	Class-D inputs	4, 5, 44, 45
	Ramp generator	6, 43, 48
	Grounds	7, 46
	Input power (VDD)	8
	Fault indicators	41, 42
12, 13, 36, 37	Output power (LPVDD, RPVDD)	9, 16, 33, 40
	Class-D outputs	10, 11, 14, 15, 34, 35, 38, 39
20	Headphone	17, 18, 19, 29, 30, 31, 32
27	Charge pump	21, 22, 23, 24, 25, 26, 28

Power plane

The chip has three main power sections: the input circuit power pins (VDD), the output stage power pins (LPVDD and RPVDD) and the power for the headphone and charge pump circuits (PVDD). When the device is fully operational, the VDD pin draws only a few milliamps of current and the PVDD pins draw several tens of milliamps, in contrast to the amps of current drawn by the LPVDD and RPVDD pins. The power traces should be kept short and the decoupling capacitors placed as close to the power pins as possible. It is important to terminate the capacitor ground close to the ground for the particular power section while paying attention to ground return current paths. This minimizes ground loops and provides very short ground return paths and high-frequency loops. The VDD pin supplies power for sensitive analog circuitry. It is the most sensitive pin of the device and must be kept as noise free as possible. The PVDD pins are not as sensitive to noise as the VDD pin and supply the current for the headphone regulator and control circuits when the device is in Class-AB mode and for the charge pump circuit when in Class-D mode. The power traces for the VDD and PVDD power inputs should be connected to the main power bus at a point near the large decoupling capacitor. The small inductance of the traces and the charge supplied by the large decoupling capacitor greatly reduce the ripple current of the main power bus at these pins. The demand for transient currents is small and is satisfied by placing 1-µF capacitors adjacent to the VDD pin and PVDD pin 21. The main power bus should terminate into the LPVDD and RPVDD pins, with a 1-µF capacitor placed adjacent to each pair of pins. A 10-µF capacitor is then placed between the power pins and the large decoupling capacitor. These traces should be symmetric and wide to facilitate even power distribution and should be directly over the ground to reduce EMI and minimize the ground return path.

Inputs and outputs

The Class-D input traces should be kept as short as possible between the ac coupling capacitors and the amplifier inputs to reduce noise pickup. The inputs must be separated from the outputs, particularly the inductors, to minimize magnetic coupling. The headphone traces may be in close proximity to the Class-D output since the two amplifiers are not active at the same time. It is critical to minimize the trace lengths between the device output pins and the LC filter components, particularly those that contain the full 250-kHz square wave. These traces should be capable of handling a maximum rms current of at least 0.7 amps without distorting the signal, and peak currents of at least 1 amp. The traces to the inductors should be kept short but separated from the input circuit as much as possible and should be placed on adjacent layers so that they overlap to reduce the EMI.

Summary

The methods described have been successfully used in the design of the TPA005D14 Class-D Audio Power Amplifier EVM, SLOP 204, providing typical THD+*N* measurements of 0.1% for a 1-kHz, 1-watt output into a 4-ohm load. Three power decoupling capacitors provide a quick, smooth response to the large current demands of the output circuit and, with proper layout, are able to supply the transients to the input circuit and charge pump. A solid ground plane is effective when components are placed close to the ground pin for their circuit, and ground and high-frequency bypass loops are minimized. EMI and distortion are greatly reduced by keeping the input traces short and ac-coupling all inputs, minimizing the output trace lengths to the filter and overlapping the output traces to the inductors of each channel on adjacent layers.

References

1. http://www.ti.com/sc/class_d.htm
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3. "PowerPAD Thermally Enhanced Package," Technical Brief, Texas Instruments Inc., literature number SLMA002; http://www-s.ti.com/sc/psheets/slma002/slma002.pdf

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